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Vanguard EMS Inc.
3725 S.W. Hocken Ave.
Beaverton, OR 97005

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11.1 COSMETIC SPECIFICATIONS
11.2 FABRICATED PARTS
11.3 ASSEMBLY DRAWINGS AND WORK INSTRUCTIONS
11.4 PACKAGING

APPENDIX A – CRITICAL ITEM DFM CHECKLIST

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1.0 Documentation Definition

1.1 Purpose

The purpose of this document is to provide design and circuit board layout information that will help maximize manufacturability and yields of circuit boards at Vanguard EMS, Inc.

This document will aid our customers in understanding Vanguard EMS assembly, test processes and manufacturing equipment requirements. This will help reduce product introduction times and reduce total manufacturing costs.

1.2 Scope

This design guide is intended to supplement, not replace existing design standards.

The information presented herein is based, in general, on IPC-7351A.

As a minimum, Vanguard EMS will perform a “Critical Item” Design for Manufacturing review for all quotes and first time builds. These Critical Items are defined in Appendix A. Appendix A also identifies potential options to resolve a violation of these “Critical Items”.

If requested by the customer or at the discretion of Vanguard EMS, a complete DFM review will be performed on an assembly, especially if the design is complex or of critical nature and provide a detailed DFM Report.

1.3 Controls

This document is internally controlled at Vanguard EMS and will need to be verified as to current level.

1.4 PCB Array Specific Requirements

The following sections are specific to the design of PCB Arrays and are applicable to customers and vendors that design arrays that will be utilized at Vanguard.

- 3.3.1 – Required Panel / PCB Features
- 3.3.2 – Recommended Panel Design
- 3.6 – Fiducial Requirements
- 4.2 – Tooling hole requirements
- 4.3 – De-Paneling/Tab Routing Guidelines
- 4.4 V-Score Panel Dimension Considerations

2.0 Board Architecture

2.1 Guidelines for Using/Designing Through-Hole and SMT

Ideally boards should be 100% SMT or 100% through-hole. Boards that use both technologies are referred to as Hybrids. The usage of through-hole parts should be minimized as much as possible. Boards that require at least two separate processes to manufacture inherently add both manufacturing time and cost. When through hole components are required Vanguard will hand install. Soldering can be accomplished via wave solder or by hand.

3.0 PCB Construction and Design

3.1 Bow and Twist

The maximum allowable bow and twist for SMT application is 0.75%, not to exceed .090”. The maximum allowable bow and twist for pure through-hole component designed PCB’s is 1%.
3.2 Plating Recommendations

The following matrix (Table 1) defines what plating finishes are best suited when specific component packages are used. They are defined by preference (1 being best).

<table>
<thead>
<tr>
<th>Condition</th>
<th>ASSEMBLY TYPE</th>
<th>SPECIFIC COMPONENT TECHNOLOGY USED</th>
<th>OSP Note 1 Note 2 Note 3</th>
<th>IM/SN</th>
<th>ENIG</th>
<th>IM / AG</th>
<th>HASL</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 100% SMT:</td>
<td>BGA, CSP</td>
<td>FINE PITCH: 16-49 MIL NO PRESS-FIT CONNECTORS</td>
<td>2 3 4 1 N/A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BGA, CSP requires flat planar mounting surfaces.</td>
</tr>
<tr>
<td>2 100% SMT:</td>
<td>NO BGA, NO CSP</td>
<td>COARSE PITCH GREATER THAN 50 MIL NO PRESS-FIT CONNECTORS</td>
<td>4 3 5 2 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Coarse pitch compatible with HASL.</td>
</tr>
<tr>
<td>3 HYBRID SMT + THROUGH HOLE:</td>
<td>BGA, CSP</td>
<td>FINE PITCH 12-49 MIL PITCH</td>
<td>3 2 4 1 N/A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BGA, CSP requires flat planar mounting surfaces.</td>
</tr>
<tr>
<td>4 HYBRID SMT + THROUGH HOLE:</td>
<td>NO BGA, NO CSP</td>
<td>COARSE PITCH GREATER THAN 50 MIL</td>
<td>4 3 5 2 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Coarse pitch compatible with HASL.</td>
</tr>
<tr>
<td>5 100% THROUGH HOLE</td>
<td></td>
<td></td>
<td>4 3 5 2 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Coarse pitch compatible with HASL.</td>
</tr>
<tr>
<td>6 100 % PRESS-FIT3</td>
<td></td>
<td></td>
<td>4 5 3 2 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HASL = ideal finish</td>
</tr>
<tr>
<td>7 HYBRID PRESS-FIT3</td>
<td>BGA, CSP, FINE PITCH 12-49 MIL PITCH WITH OR WITHOUT THROUGH HOLE</td>
<td>3 4 2 1 N/A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HASL not acceptable. Insertion lube required.</td>
<td></td>
</tr>
<tr>
<td>8 HYBRID PRESS-FIT3</td>
<td>NO BGA OR CSP</td>
<td>COARSE PITCH GREATER THAN 50 MIL WITH OR WITHOUT THROUGH HOLE</td>
<td>4 5 3 2 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HASL requires no insertion lube. All other use lube</td>
</tr>
<tr>
<td>9 LEAD FREE SOLDER REQUIREMENTS</td>
<td>ALL SMT TECHNOLOGIES WITH OR WITHOUT THROUGH HOLE NOT INCLUDING PRESS-FIT</td>
<td>3 2 1 4 N/A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LEAD FREE WITHOUT PRESS-FIT</td>
<td></td>
</tr>
<tr>
<td>10 LEAD FREE SOLDER REQUIREMENTS</td>
<td>ALL SMT TECHNOLOGIES WITH OR WITHOUT THROUGH HOLE INCLUDING PRESS-FIT3</td>
<td>3 2 1 4 N/A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LEAD FREE WITH PRESS-FIT</td>
<td></td>
</tr>
</tbody>
</table>

Table 1: PCB Plating Recommendations

OSP: Organic Solderability Preservative, ENIG: Electroless Nickel Immersion Gold, Im/Ag: Immersion Gold, Im/Sn: Immersion Tin, HASL: Hot Air Solder Level

Note 1: OSP must allow for solder deposit on all test points to meet minimum ATE probe-ability requirements.

Note 2: Solder deposit on OSP via must allow for no less than 8 mil gap between adjacent via’s. This will reduce solder bridging potential.

Note 3: For all Press-Fit applications consult connector manufacturer for finished hole size requirements and/or application requirements.

3.3 Board Construction and Fabrication
Thickness of surface mount boards should be a minimum of 0.031". Boards thinner than 0.062" will require SMT fixtures.

**Guideline**

All components **SHOULD** be marked with a reference designator and polarity indicator, if applicable, on the silkscreen. The polarity indicator **MUST** be visible after part installation. Table 2 shows the recommended reference designator location and polarity markings that should be incorporated in the silk screen.

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>IDEAL CONDITION</th>
<th>ACCEPTABLE CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Component</td>
<td>R500</td>
<td>R500</td>
<td>(No designators, missing designators)</td>
</tr>
<tr>
<td></td>
<td>R500</td>
<td>R500</td>
<td>Confusion to chip location (which pads belong to which chip)</td>
</tr>
<tr>
<td></td>
<td>R500</td>
<td>R500</td>
<td>Cannot determine designators without documentation (BOM, drawings etc.)</td>
</tr>
<tr>
<td></td>
<td>R500</td>
<td>R500</td>
<td>This condition will increase inspection cost and increase potential for wrong component loading.</td>
</tr>
<tr>
<td></td>
<td>R500</td>
<td>R500</td>
<td></td>
</tr>
</tbody>
</table>
## Design for Manufacturability Manual

**Type:** Work Instruction  
**ISO Section:** 2.0-27  
**Document #:** 11566-021  
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### COMPONENT  
**IDEAL CONDITION**  
**ACCEPTABLE CONDITION**  
**POOR CONDITION**

<table>
<thead>
<tr>
<th>Orientation and Reference Designators</th>
<th>R500</th>
<th>R501</th>
<th>R502</th>
<th>R500</th>
<th>R502</th>
<th>R501</th>
</tr>
</thead>
<tbody>
<tr>
<td>Text orientation follows device orientation.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Orientation and Reference Designators (cont.)</th>
<th>R500</th>
<th>C500</th>
<th>R501</th>
<th>R500</th>
<th>R502</th>
<th>R501</th>
<th>R500</th>
</tr>
</thead>
</table>
| Text clearly separated from adjacent devices.  
Nomenclature is consistent.  
Text orientation follows device orientation.  
Avoid silkscreen reference designators on via features.  
Small (font) devices like 0603 and smaller will become difficult (or impossible) to read when silkscreen is printed on via. |

<table>
<thead>
<tr>
<th>Polarized Capacitors</th>
<th>+</th>
<th>A</th>
</tr>
</thead>
</table>
| Mark the Anode (+) side of the capacitor silkscreen.  
Use a bar or line equal to the width of the pad. This is a “polarity indicator”. The component (generally) will have a matching line.  
Ideal polarity indicators have a mark on the board that matches the mark on the part. Though impractical for all device types, there is excellent consistency on polarized capacitors.  
Our intent is to match “alignment” |

| Unmarked polarized locations increase the complexity of the assembly process. These add delays for first article processes and can even be dangerous if polarized capacitors are mounted reversed.  
Components do not (generally) have a matching “A”. These marks (or lack of) will increase manufacturing costs and delays. |
“marks”, not necessarily interpret polarity (Anode vs. Cathode).

The highest reliability for mounting components in the correct orientation is to “match alignment marks” (part polarity identification to silkscreen mark).

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>IDEAL CONDITION</th>
<th>ACCEPTABLE CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td></td>
<td>See Ideal Condition.</td>
<td></td>
</tr>
<tr>
<td>LED’s</td>
<td></td>
<td>See Above</td>
<td></td>
</tr>
</tbody>
</table>

**COMPONENT**

**IDEAL CONDITION**

**ACCEPTABLE CONDITION**

**POOR CONDITION**

Identify the Cathode end.

Anode (A) and Cathode (C or K) or the diode symbol are extremely poor polarity indicators in manufacturing. These symbols are helpful to Test Engineering or Electrical Engineers but do not aid the manufacturing process. Utilize standard markings when ever possible.

Standard method is to identify the Cathode in the silkscreen.

Chip style SMT LED’s typically use small triangle or mark on the SMT LED as a “polarity” mark. Historically, this mark represented the Cathode. In some cases we have seen where diode manufacturers are identifying the Anode on the LED. This will cause a high likelihood of LED mis-orientation. The problem is amplified in 0603 and 0402 chip LED’s where miniaturization begins to exclude easily visible orientation features (on the LED)
**Table 2: Component silkscreen and orientation table.**

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Example</th>
<th>Observation</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOIC, SOP, SSOP etc.</td>
<td><img src="image" alt="SOIC SOP SSOP Example" /></td>
<td>Notice how the “notch” is exaggerated away from the device allowing for simple inspection after placement.</td>
</tr>
<tr>
<td>QFP, TQFP</td>
<td><img src="image" alt="QFP TQFP Example" /></td>
<td>Polarity mark is large and easily found. Cut corner should be visible when component mounted.</td>
</tr>
<tr>
<td>BGA</td>
<td><img src="image" alt="BGA Example" /></td>
<td>Silkscreen outline should be slightly larger than BGA device. Clearly visible polarity indicator.</td>
</tr>
</tbody>
</table>

Mark should be clearly visible when component is mounted.

Polarity mark is not easily recognizable.

Poor design. Atypical method is not easily recognizable.
Guideline
SMT components should be located (no closer than) 0.300 inch from the edge of the PCB. Violation of these (keep-out) clearance requirements will require the addition of edge rails to the PCB or custom fixtures (3.3.1).

Figures 1: Component Keep-out. Both Examples are acceptable

3.3.1 Required Panel / PCB features

- Any PCB exhibiting ANY violation of component keep-out regions must utilize break-away rails on ALL sides.
- Break-away rails shall measure 0.400” unless a deviation is authorized by Vanguard Engineering.
- Image PCB’s will be centered in panel frame on both axis.
- Fiducials shall be added to each panel frame in accordance with section 3.6. Fiducials shall be 0.050” ±0.010”.
- Fiducials shall not reside within 0.125” of card edge or panel frame edge.
- Panel designs shall have 0.125” +/-0.002” un-plated tooling holes located 0.196” from frame corners.
- A panel design drawing must be provided to Vanguard to allow for accurate stencil design and Pick-and-Place programming. The panel drawing must provide the following information.
  - Panel dimensions length and width.
  - Break-away rail dimensions.
  - Step-and-repeat dimensions.
  - Fiducial target dimensions and locations.
  - Tooling hole dimensions and locations.
3.3.2 Recommended panel design

A = 0.4 inch
B = image size Y-axis
C = Image size X-axis

Figure 2: Panel design requirements.

3.4 Micro Via / Via-in-pad

If via-in-pad is required in the design, then, as a minimum, the via-in-pad should be copper capped. Additionally the opposite side of the via should either be:

- Copper capped if used as a test point for ICT
- Masked or filled over to prevent entrapment of plating chemicals.

If via-in-pads are not capped, the following conditions could result in additional assembly cost:

- Solder wicking to opposite side causing paste printing issues on second pass (if via-in-pad is on the first pass side) which will result in solder bridging and solder balls
- Solder scavenging resulting in insufficient solder and voids in BGA solder balls

3.4.1 Standard Via
Clearances
Standard Via’s need to maintain minimum clearances from adjacent conductors. These clearances are a function of via type (masked or exposed). Masked vias require less clearance. Exposed vias require greater clearances to adjacent exposed conductors.

3.4.2 Via Size Guideline
Table 3 lists the recommended Via size guidelines. For Type II attach methods there must be a .025” diameter area free of vias at the centroid of each passive device on the secondary side as shown in Figure 4. Vias placed in this region “rob” adhesive, which makes it difficult to bond the device to the board for wave solder. This design rule is only valid on Type II designs that use epoxy attach methods for wave solder immersion.

<table>
<thead>
<tr>
<th>Via Type</th>
<th>Outside Ring Diameter</th>
<th>Hole Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>.030”</td>
<td>.020”</td>
</tr>
<tr>
<td>Alternative</td>
<td>.020”</td>
<td>.013”</td>
</tr>
<tr>
<td>Alternative</td>
<td>.018”</td>
<td>.011”</td>
</tr>
<tr>
<td>Test Point</td>
<td>.035”</td>
<td>.020”</td>
</tr>
</tbody>
</table>

Table 3: Via Size Guideline

3.4.3 Masked Vias:
Masked vias are preferred. This method should be employed as a default design method. Masked vias offer the greatest resistance to solder bridges or shorts.

3.4.4 Exposed Vias:
Exposed vias are not covered in solder resist (mask). These are exposed conductors which, in certain circumstances, can allow solder shorts to occur. Clearances for exposed vias are dictated by adjacent artwork features.
3.4.5 Rules for Masking Vias under BGAs

It is Preferred that BGA via's be masked as a default design rule. Masked vias are the best method to prevent solder shorts under BGA's.

Chip Components

Chip components can shift or skew during the reflow process. This can cause the component termination to short across to adjacent exposed conductors (vias). Therefore, the via “keep-out” spacing is dictated by the component termination width. See Figure 6 from good design practices for vias associated with chip components.

Exposed Via Location Rule: Adjacent to SMT pads. Exposed vias should be a minimum of 50% component termination width + 0.020 inch. This will ensure chip component shift / skew will not create a solder short.

Exposed Via Location Rule: End of SMT pads. Minimum clearance 0.020 inch from exposed conductors.

Figure 6: Pad Isolation techniques
### Table 4: Exposed via locations.

#### 3.5 Runs & Ground Planes

**Guideline**

All ground/power planes should be internal to the board and located symmetrically about the center of the thickness. This will minimize the board from warping.

**Guideline**

All traces should be as equally distributed as possible in both the X and Y directions and should not be oriented in only a single direction on each layer. This will minimize the board from warping.
3.6 Fiducial Requirements

Fiducials are required for manufacturability, and fiducial registration is the primary SMT manufacturing registration method.

It is recommended that the Fiducials conform to the illustrations shown in Table 5. Fiducial target diameter may range in size ±0.010". Deviation from this requirement could prevent the SMT vision system from properly aligning the PCB.

Solder mask isolation is required. Omission of this feature will reduce the accuracy of Vanguard’s SMT placement equipment and increase delays. Holes or land patterns should never be considered as registration marks. Land patterns are often covered with solder paste and rendered unusable to the SMT vision system. Through-holes or vias are poor choices (as fiducials) due to the fact that drill wander causing hole tolerances that are significantly greater than lithographic etch processes used for copper artwork. Fiducials are purpose built artwork features and are mandatory to standard manufacturing strategies.

<table>
<thead>
<tr>
<th>Ideal</th>
<th>Acceptable</th>
<th>Not Acceptable</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Fiducial Camera Field-of-View (FOV)" /></td>
<td><img src="image" alt="Fiducial Camera Field-of-View (FOV)" /></td>
<td><img src="image" alt="Fiducial Camera Field-of-View (FOV)" /></td>
</tr>
<tr>
<td>Fiducial Target 0.050 +/- 0.010 inch</td>
<td>Fiducial Target Clearance. No Solder Resist or glassification allowed. Diameter = 0.157 in. (3.8 mm) (2X -3X Fiducial Diameter)</td>
<td><img src="image" alt="R501 Via" /></td>
</tr>
<tr>
<td>Fiducial scan area must be void of all art-work features 0.196 in (5mm)</td>
<td>Problems: 1. Fiducial target clearance (Keep-out) less than 2 times fiducial diameter. 2. Artwork Features enter into the Fiducial Scan Area. 2 Test pads, 1 Via and R501 silk-screen can interfere with our manufacturing equipment fiducial recognition</td>
<td></td>
</tr>
</tbody>
</table>

**Table 5: Fiducial Design**

Fiducials shall be located in the corners of each image and in three of the corners of the panel. Fiducials should be located as far apart as possible and should be in the same plane on each axis.
3.7 Polyimide flex and rigid flex assemblies

Flex assemblies introduce another variable to manufacturing. The flexible nature of the Polyimide coupled with its minimal thickness will require a supporting fixture through the SMT manufacturing process. Rigid flex assemblies, depending on configuration, may require special considerations. These special considerations often are design dependent.

Recommendations:

1. Fiducial features are required.
2. Keep all SMT to a single side.
3. Tooling holes (locating holes) cannot be used on materials thinner than 0.031 inch. The tooling pins interfere with the solder printing process.
4. No-clean process is preferred. Type I or Type II assembly should employ no-clean flux. Water soluble process will require a bake-out process between the first SMT pass and the second SMT pass. This is to prevent de-lamination but adds significant delays to the assembly process.

5. Polyimide is extremely hydroscopic and is dimensionally unstable. Typical growth is 1 - 3%. This undesirable attribute will affect mounting accuracies.
   a. Restrict passive components to no smaller than 0603.
   b. Active (I.C’s) to greater than 0.65mm pitch
   c. Devices with pitch smaller than 0.65mm must use a local fiducial.

6. Do not select snap-in devices for use with flex assemblies (Example: RJ45 connectors, Mictor staked connectors etc.)

7. Snap in or staked devices are acceptable for rigid assemblies. However, if a double sided SMT attach is required, the stakes must not protrude.

8. Overhanging devices on rigid only assemblies should employ strain relief. Use of (integrated) solder tabs or adhesive (attachment) is preferred. Failure to utilize strain relief can result in lifted solder lands.

9. Use of panelized flex assemblies should employ minimalist strategies. Larger is not necessarily better with flex assemblies. Panel design is design-specific. Consult with Vanguard Engineering.

10. Rigid flex assemblies should consider a built-in strain relief when using buried flex layer or when Polyimide is less than 0.010 inch. This is to prevent a “fold” or shear point, which will crack the copper conductors.

11. Flex / Rigid flex assemblies should consider purpose built packaging to prevent folding of the Polyimide and subsequent component damage.

12. With rigid/flex designs, a minimum of 0.3 inches (prefer 0.4 inches) between board images. This is needed for the fabrication vendor to manually adjust the flex material prior to press. This spacing will also depend on the design.

13. With rigid/flex designs, tabs are the preferred method of keeping the image attached to panel. V-score is possible but it will mean an extra step either at the fabrication or manufacturing process to cut the flex material.

### 4.0 Dimensional Considerations

#### 4.1 Maximum board profile with Components

The board size Vanguard EMS is capable of processing is dictated by the types of processes required to assemble the PCB. (ALL UNITS IN INCHES)

<table>
<thead>
<tr>
<th>PROCESS</th>
<th>MINIMUM SIZE</th>
<th>MAXIMUM SIZE</th>
<th>THICKNESS (MIN.)</th>
<th>THICKNESS (MAX.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMT</td>
<td>2 X 2</td>
<td>18 X 16</td>
<td>0.010</td>
<td>0.196</td>
</tr>
<tr>
<td>AOI</td>
<td>2 X 2</td>
<td>23.6 X 23.6</td>
<td>0.010</td>
<td>0.196</td>
</tr>
<tr>
<td>AQUEOUS WASH (WITH BASKET)</td>
<td>NONE</td>
<td>19-1/8 X 19-1/8</td>
<td>NONE</td>
<td>2-1/16</td>
</tr>
<tr>
<td>AQUEOUS WASH (NO BASKET)</td>
<td>5 X 5</td>
<td>23 INCH WIDTH</td>
<td>0.010</td>
<td>2.5</td>
</tr>
<tr>
<td>OA WAVE SOLDER</td>
<td>2 X 2</td>
<td>17 X 20</td>
<td>0.031</td>
<td>0.196</td>
</tr>
<tr>
<td>NO-CLEAN WAVE SOLDER</td>
<td>2 X 2</td>
<td>15 X 18</td>
<td>0.031</td>
<td>0.196</td>
</tr>
<tr>
<td>LEAD FREE, NO-CLEAN WAVE SOLDER</td>
<td>2 X 2</td>
<td>15 X 18</td>
<td>0.031</td>
<td>0.093</td>
</tr>
<tr>
<td>PRESS-FIT</td>
<td>2 X 2</td>
<td>24 X 48</td>
<td>0.062</td>
<td>0.3937</td>
</tr>
</tbody>
</table>

* Larger sizes are available for small prototype batch production. Contact Vanguard directly for specifications.
4.2 Tooling Holes

Two tooling holes per image within a PCB are needed for registration of board for ICT test. Recommended hole sizes are 0.125 ±0.002". Tooling holes should be un-plated. The area over the tooling holes should be free of mechanical interference to a height of 1” inch. The positional tolerance from tooling hole to tooling hole, center to center, should be +0.004" / - 0.000". Tooling holes should be placed 0.196" x 0.196” (same axis) from the corners of the PCB.

4.3 De-paneling/Tab Routing Guidelines

Board assemblies can be de-tabbed at Vanguard EMS using perforated breakaway tabs, v-groove breakaway tabs or hand cutting with a de-tabbing tool. These guidelines will reduce board damage or scrap for the de-paneling process. Following these guidelines will help prevent damage to both components and the board during de-paneling and prevent flooding during the wave solder process.

All designs must have SMT components placed a minimum of 0.100" from the board edge. All other features (runs, vias, through hole components, etc.) must have a minimum of 0.050” clearance from the board edge. Figures 8.1 and 8.2 shows the preferred PCBA design for SMT and through hole to PCB edge clearance for de-panelization, along with the manufacturing risk level when the recommended clearance is not maintained.

Break-away designs should have perforation holes that are typically spaced at 0.050” intervals. The location of the breakaway edge will affect the smoothness of the edges.

The slightly inset version is preferred because it will require the least amount of additional labor to clean up. Tabs are typically spaced 3” on center (not to exceed 4.0”). Place tabs approximately 1.00” from corners to reduce sagging during reflow or wave soldering. It is desirable to have at least one tab per side. Figure 9 shows Vanguard’s preferred break-away tab design.

---

2 PCB thickness has a +/- tolerance. Maximum thickness must not be exceeded.

Table 6: Board size capabilities.
Figure 8.1: Tab clearance.

<table>
<thead>
<tr>
<th></th>
<th>Preferred</th>
<th>Acceptable</th>
<th>**Conditional</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Clearance</td>
<td>0.100&quot;</td>
<td>0.070&quot;</td>
<td>Less than 0.070&quot;</td>
</tr>
<tr>
<td><strong>Conditional</strong></td>
<td></td>
<td></td>
<td><strong>No tabs shall be within .750&quot; along the route cut axis to the nearest SMT pad edge or component body.</strong></td>
</tr>
<tr>
<td>Manufacturing Risk</td>
<td>Lowest</td>
<td>Higher</td>
<td>Highest</td>
</tr>
</tbody>
</table>
Figure 8.2: V-score clearance.

<table>
<thead>
<tr>
<th></th>
<th>Preferred</th>
<th>Acceptable</th>
<th>Poor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Clearance</td>
<td>0.100&quot;</td>
<td>0.050&quot;</td>
<td>Less than 0.050&quot;</td>
</tr>
<tr>
<td>Manufacturing Risk</td>
<td>Lowest</td>
<td>Higher</td>
<td>Highest</td>
</tr>
</tbody>
</table>

Increasing component distances to break-away will reduce de-panel stresses on components. Clearances of less than 0.070 should only be used where ultra-miniaturization is required. On tab routed PCB’s, hand placement and the hand soldering of these type of components after panel removal may be another option.
NOTE: Vanguard Engineering will determine where to locate break line base on fab design.
Edge Routing Guideline
Use .093” routed slots as a minimum, for single image panels. Use .125” routed slots, when two boards or more are in a panel, to allow for more accurate edge dimensions.

Edge Rail Guideline
Parallel surfaces are required for a PCB to be processed in through an SMT line. This is to prevent skewing through the conveyor system. All odd shaped PCB’s MUST have edge rails incorporated to meet this requirement. Custom reflow fixtures would have to be developed if this requirement is not met. See Section 4.4 for recommendations.

4.4 V-score panel dimensional considerations.

All V-score lines should follow the 1/3 rule illustrated in Figure 10.
Minimum thickness PCB = 0.032”
Maximum thickness PCB = 0.110”
Maximum V-score de-panel length = 18 inches
4.5 Component orientation and panel break-away.

Figure 10: V-score 1/3 rule diagram
ORIENT SHORTEST COMPONENT AXIS PERPENDICULAR TO DEPANEL (SHEAR) AXIS.

0.100 INCH (MIN.)

POOR

PREFERRED

SHEAR AXIS

Figure 11: Component orientation vs. shear axis
4.6 Panel design using V-score

The recommended panelization for v-score PCBAs is shown in Table 8

<table>
<thead>
<tr>
<th>Ideal Condition</th>
<th>Poor Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Ideal Condition Diagram" /></td>
<td><img src="image2" alt="Poor Condition Diagram" /></td>
</tr>
<tr>
<td>COMPLETE SCORE LINE</td>
<td>Low strength design. Susceptible to accidental breakage during manufacturing.</td>
</tr>
<tr>
<td>JUMP SCORE LINE</td>
<td>Will &quot;bow&quot; significantly in reflow process rendering difficulty on inverted (second)</td>
</tr>
<tr>
<td>PANEL IMAGE FRAME</td>
<td></td>
</tr>
<tr>
<td>INDIVIDUAL PCB IMAGES</td>
<td></td>
</tr>
</tbody>
</table>

Uses standard singulation equipment.

Horizontal PCB rails use full score method. All others use jump score.

Panel frame offers good strength throughout the manufacturing process.

Table 8 Panel design using v-score
4.7 **Manufacturability vs. Form factor.**

Table 9 shows the desired panelization to obtain the ideal manufacturability of a PCBA.

<table>
<thead>
<tr>
<th>PCB Condition</th>
<th>IDEAL CONDITION</th>
<th>ACCEPTABLE CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallelism</td>
<td>All opposite sides are parallel.</td>
<td>Two opposite sides are parallel</td>
<td>No opposite sides are parallel</td>
</tr>
<tr>
<td>Keep-Out Violations</td>
<td>Any PCB that has ANY violation of component keep-out will utilize break-away rails on ALL sides.</td>
<td>See Ideal</td>
<td>See Ideal</td>
</tr>
</tbody>
</table>

**Square Key**

- COMPONENT FREE
- AVAILABLE COMPONENT REAL ESTATE

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SQUARE</td>
<td>SQUARE</td>
<td>SQUARE</td>
</tr>
</tbody>
</table>

Keep out area on 4 sides offers maximum flexibility to the manufacturing process.

Parallel sides = ideal condition. Require two pairs of parallel sides with no interruptions or voids along perimeter.

Easily stacked in card carriers.

Two parallel sides with component keep-out. Require two pairs of parallel sides with no interruptions or voids along perimeter.

Can be stacked in card carriers. However, components may come in contact with carrier. This carries a risk for component damage.

No component keep-out will require the use of break-away rails, full panel frame or fixtures. Fixturing condition = low manufacturability and increased cost.

Cannot be stacked in card carriers. Poor movement efficiency on factory floor.

**Rectangle**

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RECTANGLE</td>
<td>RECTANGLE</td>
<td>RECTANGLE</td>
</tr>
</tbody>
</table>

Acceptable only if length to width aspect ratio is less than 1.4

No component keep-out will require the use of break-away rails, full panel frame or fixtures.

**Coupon fill regions and slots / voids**

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>COUPON FILL</td>
<td>COUPON FILL</td>
<td>COUPON FILL</td>
</tr>
</tbody>
</table>

All boards that are not “regular polygons” should utilize a full frame.

Board voids should be filled with a coupon if wider than 0.125 inch.

Slots or router (voids) should be no wider than 0.125 inch. There are no restrictions on length.

Following these recommendations allows for the maximum flexibility on the manufacturing line and will prevent equipment optical sensor malfunction and special equipment programming.

No component, keep-out plus large PCB void will require the use of break-away rails, full panel frame or fixtures.
4.8 SMT Pallet Considerations

a. Figure 12 illustrates the designed SMT pallet design.
b. Pallet including the board must not weight more than 2.0Kg. (4.4 lbs.)
c. SMT Pallet must use reflective surface on the underside (facing down) to allow for proper operation of IR optical sensors.
d. Pallets (fixtures) will utilize tooling holes in all 4 corners. All holes will be 5 mm x 5 mm from the corners.
e. Clearance perimeter by 2 inches. Features may extend no more than 0.5 inch below top side of fixture in this keep-out area.
4.9 Form Fit and Function Considerations
Form, Fit or Function conditions will default to IPC-A-610-D (which states): “Conditions that are not specified as defective or as a process indicator may be considered acceptable unless it can be established that the condition affects user defined form, fit or function.”

Any condition determined as non-compliant under Form, Fit or Function will have its requirements specified as “user defined” aka “customer requirements”. It is mandatory that these customer requirements are identified on: customer drawings, BOM, ECN, Temporary Deviations or specification sheets.

5.0 Component Placement, Spacing and Orientation

5.1 Termination
Only a single lead or termination should be placed on a land. Use Solder Mask Defined pads. Placing two or more lead terminations on a single land (See Figure 13), causes:
   a. Unpredictable solder flow.
   b. Component skewing
   c. Increased occurrences of “tombstoning” and “draw-bridging” defects.

5.2 Component Spacing
Definition: Spacing refers to the gap between adjacent conductors. Typical pad designs are larger than component terminations or leads. Therefore the isolation required between conductors (pads) will be considered.

Tables 11a – 11c illustrates the recommended minimum spacing between various SMD components based on the SMT density.
NOTE:
*1 Standard Clearance = 250 mils. This clearance offers the greatest manufacturing flexibility possible. Co-planarity will determine if a step solder paste stencil is required. Refer to section 5.2.1 for exact clearance requirements.
*2 Reducing these clearances below 0.100 inch will increase complexity of any subsequent rework operations.
*3 RULE: Chip-to-Chip spacing rules.

<table>
<thead>
<tr>
<th>Manufacturable</th>
<th>Less Manufacturable</th>
<th>Difficult to Manufacture</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
<td><img src="image3" alt="Diagram" /></td>
</tr>
</tbody>
</table>

Table 10: Component spacing rules.
### Design for Manufacturability Manual

**Type:** Work Instruction  
**ISO Section:** 2.0-27

**Document # 11566-021**  
**Page 31 of 54**

#### Conventional Designs

<table>
<thead>
<tr>
<th>CHIP</th>
<th>TANTALUM</th>
<th>SMALL OUTLINE</th>
<th>QFP</th>
<th>SOT23</th>
<th>PLCC</th>
<th>BGA ¹</th>
<th>CSP ¹</th>
<th>CBGA ¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP</td>
<td>Note 3</td>
<td>60</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>250</td>
<td>250</td>
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<td>75</td>
<td>100</td>
<td>250</td>
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<td>SO</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>100</td>
<td>50</td>
<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>QFP / TSOP / VSOP</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>SOT23</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>100</td>
<td>40</td>
<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>PLCC</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>BGA ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
</tr>
<tr>
<td>CSP ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
</tr>
<tr>
<td>CBGA ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
</tr>
</tbody>
</table>

*Table 11a: Conventional Component spacing (dimensions are in mils)*

#### High Density Designs

<table>
<thead>
<tr>
<th>CHIP</th>
<th>TANTALUM</th>
<th>SMALL OUTLINE</th>
<th>QFP</th>
<th>SOT23</th>
<th>PLCC</th>
<th>BGA ¹</th>
<th>CSP ¹</th>
<th>CBGA ¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP</td>
<td>Note 3</td>
<td>50</td>
<td>40</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>250</td>
<td>250</td>
</tr>
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<td>TANTALUM</td>
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<td>50</td>
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<td>100</td>
<td>75</td>
<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>SO</td>
<td>40</td>
<td>55</td>
<td>50</td>
<td>75</td>
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<td>250</td>
</tr>
<tr>
<td>QFP / TSOP / VSOP</td>
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<td>75</td>
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<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>SOT23</td>
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<td>50</td>
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<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>PLCC</td>
<td>50</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>BGA ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
</tr>
<tr>
<td>CSP ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
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<tr>
<td>CBGA ¹</td>
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<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
</tr>
</tbody>
</table>

*Table 11b: High density component spacing (dimensions are in mils)*

#### Ultra High Density Designs

<table>
<thead>
<tr>
<th>CHIP</th>
<th>TANTALUM</th>
<th>SMALL OUTLINE</th>
<th>QFP</th>
<th>SOT23</th>
<th>PLCC</th>
<th>BGA ²</th>
<th>CSP ²</th>
<th>CBGA ¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP</td>
<td>Note 3</td>
<td>35</td>
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<td>250</td>
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<td>TANTALUM</td>
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<td>75</td>
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<td>250</td>
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<tr>
<td>SO</td>
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<td>50</td>
<td>50</td>
<td>75</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>QFP / TSOP / VSOP</td>
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<td>50</td>
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<td>75</td>
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<td>250</td>
</tr>
<tr>
<td>SOT23</td>
<td>30</td>
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<td>30</td>
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<td>250</td>
</tr>
<tr>
<td>PLCC</td>
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<td>75</td>
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<td>75</td>
<td>50</td>
<td>100</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>BGA ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>100</td>
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</tr>
<tr>
<td>CSP ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>75 ¹</td>
<td>100</td>
<td>100</td>
</tr>
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<td>CBGA ¹</td>
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<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
<td>250 ¹</td>
</tr>
</tbody>
</table>

*Table 11c: Ultra high density Component spacing (dimensions are in mils)*

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5.2.1 Component keep-out clearances vs. device co-planarity:

Typical SMT stencil thickness is 5 mils. This encompasses standard device types of 0402, 0603 chip resistors / capacitors even 0.5mm fine pitch. However, if any device co-planarity exceeds the thickness of the stencil (which determines the height of the solder paste brick) then an open solder joint will be created. To combat this defect it is possible to use step-stencil architecture. Step stencils are stencils that have specific regions that use thicker foil to create deeper solder deposits. For example a standard 5 mil stencil foil can have a device type “stepped” up to 8 mils. to allow for increased deposition of solder paste.

There are two methods we use for stepping stencils.
1. Lamination or additive process.
2. Etch away or subtractive process.

Both methods will yield the same results of selective deposition to combat co-planarity issues in components or increased solder volume requirements. Consequently, both step processes are applied in a “step facing down method”. This method prevents metal squeegee damage and offers the most accurate and repeatable printing method.

Typical devices that may require a step stencil are:
- Ceramic BGA (CBGA) devices that use high temperature balls (Pb90 / Sn10). Typical ball-to-ball co-planarity may range between 6 to 8 mils*
- Pin Grid Array sockets or BGA adaptors. Rigid pin designs often have up to 10 mils* of co-planarity. Floating pin designs 5 to 8 mils*
- How to calculate component Keep-out:
  1. Determine device co-planarity. Use ball-to-ball or lead-to-lead method.
  2. Select Column “Coplanarity is” for your co-planarity specification. Move down 1 row to the “Use” specification.
- See Table 12 for recommended keep out sizes
*Coplanarity is device specific. Consult manufacturers’ data sheet.
5.3 Component Orientation

The geographic location of a component on a PCB can impact the manufacture ability of the board. The following are guidelines that should be considered for ease in assembly.

- BGA’s should only be placed on the topside of the PCB. This eliminates the possibility of open solder connections due to the weight of the part during second pass reflow. An added process step would be required to temporarily support the secondary side BGA’s during the second pass reflow process.

- BGA’s and larger QFP devices (> than 100 leads) should not be placed in the center of the PCB. The maximum board warpage tends to be in the center of the PCB. The result can be open solder connections. For a standard .062” PCB, this becomes a concern when the surface area exceeds 25 in².
• If BGA’s are on both sides of the board, it is not recommended that the BGA’s are positioned on top of each other (See Table 13). This method makes rework of a BGA extremely difficult. In addition, this method makes x-ray inspection of the solder balls of the BGA very difficult.

**Figure 15: Example of Effect of bow-and-twist on BGA devices.**

<table>
<thead>
<tr>
<th>IDEAL CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET MOUNT</td>
<td>MIRROR MOUNT</td>
</tr>
<tr>
<td>PCB SUBSTRATE</td>
<td>PCB SUBSTRATE</td>
</tr>
<tr>
<td>Simple rework methods used.</td>
<td>Rework of defective device may negatively affect mirrored device.</td>
</tr>
<tr>
<td>Open architecture often advantageous for debug and testing.</td>
<td></td>
</tr>
</tbody>
</table>

*Table 13: BGA mounting strategy.*

• All polarized surface mount or through hole components should be placed in the same orientation and in only one axis. This facilitates ease in visual inspection.

**5.3.1 Chip Under Device**

Recommendations when employing chip under device:

• Chip under Dram or other device types can complicate inspectability, rework and device testing.

• Keep device thickness tolerance and process stack-up tolerances in mind when specifying chip under device.

• SMT solder has thickness. This dimension should be accounted for in the design. Typical device-to-pad gap is 2-3 mils.
Devices placed under BGA sockets, chip carriers or ZIF sockets need to account for BGA ball collapse. Collapse is typically 20-30% of the ball diameter. However, the weight (density) of the ZIF and type of solder composition can affect the final clearance height. Keep stack-up tolerances in mind with these types of designs. This type of design practice is extremely risky due to:

1. Inability for AOI or manual inspection of hidden devices.
2. Extreme difficulty for rework on hidden devices due to device failure or manufacturing defect.
3. Test access may become limited.

The highest degree of manufacturability exists when proper courtyard spacing is utilized.

### 5.4 SMD Size Requirements and Capabilities

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Production</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0201</td>
<td>Yes</td>
<td>5,000 per board max.</td>
</tr>
<tr>
<td>0402</td>
<td>Yes</td>
<td>15,000 per board max</td>
</tr>
<tr>
<td>Micro BGA</td>
<td>0.4, 0.5, 0.8 mm</td>
<td>Less than 54mm²</td>
</tr>
<tr>
<td>PBGA</td>
<td>1.0, 1.27, 1800 balls</td>
<td>Less than 54mm²</td>
</tr>
<tr>
<td>CBGA</td>
<td>1.0, 1.27, 1800 balls</td>
<td>Less than 54mm²</td>
</tr>
<tr>
<td>QFN / CSP</td>
<td>32 – 128 I/O, 0.5mm pitch</td>
<td></td>
</tr>
<tr>
<td>Fine Pitch</td>
<td>15.8 – 20 mil pitch up to 304 I/O</td>
<td>Capable to 12 mil</td>
</tr>
<tr>
<td>CLCC</td>
<td>Yes</td>
<td>Less than 54mm², not to exceed 80 grams</td>
</tr>
<tr>
<td>Tray Components</td>
<td>50 stock numbers, 150 trays total</td>
<td></td>
</tr>
</tbody>
</table>

*Table 14: SMD size and capabilities.*

#### 5.4.1 Resistor Pack (R-Pack) Limitations

Resistor Packs also called R-Packs or Resistor Networks have critical design features that can limit the manufacturability of a PABA and add additional rework time. To improve manufacturability and to limit the number of solder defects associated with resistor packs, it is preferred that the design incorporates resistor packs with Convex type terminations and external solder joints. Convex terminations with external solder joints on resistor packs provide a better surface for improved solder joints and provide easier access to the solder joints for inspection and if necessary rework.

PCBA designs than incorporate resistor packs that incorporate other designs such as castellation-type packages are prone to latten terminal plating issues, solder defects and undetectable internal hairline cracking that cannot be detected.

#### 5.4.2 Thermal Process Requirements for SMD and Through Hole Components (Reflow and Wave Solder)

**Surface Mount:**  
SnPb Eutectic Process – Package Classification Peak Reflow Temperatures:  

<table>
<thead>
<tr>
<th>Package Thickness</th>
<th>Volume mm³ &lt;350</th>
<th>Volume mm³ ≥350</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;2.5mm</td>
<td>240 +0/-5 °C</td>
<td>225 +0/-5 °C</td>
</tr>
<tr>
<td>≥2.5mm</td>
<td>225 +0/-5 °C</td>
<td>225 +0/-5 °C</td>
</tr>
</tbody>
</table>

*Table 15: SnPb Eutectic process – package classification reflow temperatures.*

Pb-Free Process – Package Classification Reflow Temperatures  
### Design for Manufacturability Manual

**Type:** Work Instruction  
**ISO Section:** 2.0-27  
**Document #:** 11566-021  
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---

#### Table 16: Lead-free process – package classification reflow temperatures

<table>
<thead>
<tr>
<th>Package Thickness</th>
<th>Volume mm³</th>
<th>Volume mm³</th>
<th>Volume mm³</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt;350</td>
<td>350 - 2000</td>
<td>&gt;2000</td>
</tr>
<tr>
<td>&lt;1.6 mm</td>
<td>260 +0 °C</td>
<td>260 +0 °C</td>
<td>260 +0 °C</td>
</tr>
<tr>
<td>1.6 mm – 2.5 mm</td>
<td>260 +0 °C</td>
<td>250 +0 °C</td>
<td>245 +0 °C</td>
</tr>
<tr>
<td>≥2.5 mm</td>
<td>250 +0 °C</td>
<td>245 +0 °C</td>
<td>245 +0 °C</td>
</tr>
</tbody>
</table>

---

**Sn-Pb Classification Reflow Profile**

- **Ts max**
- **Ts min**
- **TL (Liquidous) = 183 °C**
- **T P**
- **Time Above Liquidous (TAL) = 60-150 sec.**
- **25 °C to Peak = 4 min. max.**
- **Ramp-up:** 3 °C/second max.  
- **Ramp-down:** 6 °C/second max.  
- **Preheat:** 60-120 sec.

---

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Figure 16: IPC-0020C Classification reflow profiles for tin-lead and lead free solders.

Table 17: Classification reflow profile.

<table>
<thead>
<tr>
<th>Profile Feature</th>
<th>Sn-Pb Eutectic Assembly</th>
<th>Pb-Free Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Ramp-up rate (Ts(_{\text{max}}) to T(_p))</td>
<td>3 °C/ Second maximum</td>
<td>3 °C/ Second maximum</td>
</tr>
<tr>
<td>Preheat</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Min (Ts(_{\text{min}}))</td>
<td>100 °C</td>
<td>150 °C</td>
</tr>
<tr>
<td>Temperature Max (Ts(_{\text{max}}))</td>
<td>150 °C</td>
<td>200 °C</td>
</tr>
<tr>
<td>Time (Ts(<em>{\text{min}}) to Ts(</em>{\text{max}}))</td>
<td>60-120 seconds</td>
<td>60-180 seconds</td>
</tr>
<tr>
<td>Time maintained above (liquidous) Temperature (T(_L))</td>
<td>183 °C</td>
<td>217 °C</td>
</tr>
<tr>
<td>Time (t(_L))</td>
<td>60-150 seconds</td>
<td>60-150 seconds</td>
</tr>
<tr>
<td>Peak Classification Temperature (T(_p))</td>
<td>See Table 15</td>
<td>See Table 16</td>
</tr>
<tr>
<td>Time within 5 °C of actual Peak Temperature (t(_p))</td>
<td>10-30 seconds</td>
<td>20-40 seconds</td>
</tr>
<tr>
<td>Ramp-Down Rate</td>
<td>6 °C/second maximum</td>
<td>6 °C/second maximum</td>
</tr>
<tr>
<td>Time 25 °C to Peak Temperature</td>
<td>6 minutes maximum</td>
<td>8 minutes maximum</td>
</tr>
</tbody>
</table>

Wave Solder Thermal Process:

<table>
<thead>
<tr>
<th></th>
<th>Sn-Pb</th>
<th>Pb-Free</th>
</tr>
</thead>
<tbody>
<tr>
<td>Immersion in Bath</td>
<td>Components must be specified for a minimum</td>
<td>Components must be specified for a minimum</td>
</tr>
<tr>
<td></td>
<td>temperature of 475 °F for a minimum of 4 seconds</td>
<td>temperature of 525 °F for a minimum of 4 seconds</td>
</tr>
</tbody>
</table>
Through Hole Components

**GUIDELINE**
Axial leaded components are preferred over radial leaded components. Directional package style is preferred over bi-directional. This prevents components from being miss-orientated.

Hole Size requirements. Use Table 19 for determining Plated Through Hole (PTH) finished sizes. Use column A to maximize hole tolerances and manufacturability whenever possible.

- PTH too large: Components will “jump” out of board during handling, have reduced parallelism / perpendicularity or increased component lift, may not allow for a topside fillet (inspection aid), flood the topside of the board with solder (from the wave solder machine) creating solder shorts.
- PTH too small: Interference fit may not allow component to fit PTH, may not allow for proper ultrasonic spray fluxing clearances (resulting in insufficient solder fill).

<table>
<thead>
<tr>
<th>Designed for immersion in solder bath.</th>
<th>Designed for immersion in solder bath.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Plated Through Holes (PTH)</strong></td>
<td><strong>Component leads must be capable of a minimum temperature of 475 °F for a minimum of 4 seconds</strong></td>
</tr>
<tr>
<td><strong>Component leads must be capable of a minimum temperature of 525 °F for a minimum of 4 seconds</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Top-Side Pre-Heat</strong></td>
<td><strong>Typical Preheat temperatures are 160-260°F. Components must be capable of surviving these pre-heat temperatures.</strong></td>
</tr>
<tr>
<td><strong>Typical Preheat temperatures are 200-300°F. Components must be capable of surviving these pre-heat temperatures.</strong></td>
<td></td>
</tr>
</tbody>
</table>

*Table 18: Wave solder thermal process.*
5.6 Thermal Isolation

Thermal isolation is critical to hand soldering, wave soldering and SMT processes. This is especially true on multi-layer, high copper content assemblies. Without this isolation it becomes difficult to maintain process temperatures in the soldering areas of the assembly. The idea here is to slow the rate of heat sinking out of the PTH through the use of isolation (artwork). Utilize IPC-275 where ALL layers contact PTH barrels.

Good isolation techniques yield:
- a. More complete PTH (barrel) fill with solder.
- b. Solder joint inspection is faster / easier.
- c. Greater manufacturability, improved reliability

Poor isolation techniques yield:
- a. Incomplete barrel fill.
- b. Greater difficulty in inspection because of no fillet. No fillet = difficulty in determining barrel fill.
- c. Less manufacturability, lower reliability.

5.7 Bar-Code Labels

Bar code labels are added to all assemblies to provide real-time tracking and traceability. Labels can be temporary or can be a permanent fixture of the assembly. Permanent labels are preferred. However, this will require a space on the PCB surface for label attachment.
Label requirements:

Label size is 0.9 x 0.25 inch. Label is 2.5 mil +/- 1.0 mil. Label can survive up to 350 Celsius for 80 seconds. Clearance around the label is a function of surrounding components. Label must remain visible on PCB assembly throughout assembly process.

<table>
<thead>
<tr>
<th>Label Clearance</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal</td>
<td>0.25 inch From fine pitch / Micro BGA, 0201, 0402, QFN devices.</td>
</tr>
<tr>
<td>Acceptable</td>
<td>0.1 inch 1.0, 1.27mm BGA, 0603 devices or larger.</td>
</tr>
<tr>
<td>Acceptable</td>
<td>0.050 inch Through hole devices</td>
</tr>
</tbody>
</table>

Table 20: Bar code label clearance requirements

6.0 Double Sided Boards

6.1 Back side Wave Soldering (Type II or Type III Assemblies)

Boards designed as double-sided assemblies with components wave soldered on the secondary (back) side. This method is typically only preferred for short production runs. They require special design rules.

The minimum spacing shown below of .025" land to land perpendicular to the solder direction and .025" land to land parallel to the solder direction MUST be maintained to avoid wave solder defects (bridging). The minimum spacing from the edge of the annular ring of through-hole component pads or vias to a surface mount land or another via is .025".
Figure 17: Chip-in-wave minimum component clearances.

All components used on the wave solder sides of an assembly MUST be approved for immersion in a solder bath.

Components taller than .100” (typically tantalum caps or inductors) require .100” clearance land to land in all directions to prevent solder defects (skips and opens) during the wave solder operation. Components or leads are limited to .125” in height or length to clear the solder pot nozzle in the wave solder machine.
6.2 Back Side Wave Soldering (Type II or Type III Assemblies, continued)

Components that cannot be placed on the backside are as follows:

- BGA components
- CSP components
- QFP components
- "J" leaded devices
- Connectors
- Any device that cannot be submerged in solder.
- Non-encapsulated inductors

6.3 Selective Wave Soldering

Preferred method for processing mixed technology boards. The DFM requirements for this process are different than that of section 6.1. SMD components on the backside of the PCB are reflow soldered. A custom wave solder fixture shields the SMD components from being submerged in to solder. Only the through hole components are left exposed for wave soldering.

The clearance required on the backside of the board from the edge of a through-hole lead is .125". This is to allow sufficient space for the wave solder fixture to shield the SMD components as well as enough clearance to break the surface tension of the solder and allow it to make contact with the through-hole lead. A reduction in clearance will impact the wall thickness of the fixture and/or create a shadowing effect resulting in "open" solder connections.
Figure 18: Mixed Technology component clearances for selective soldering.
Additionally, thinner wall dimensions will reduce the total life expectancy of the solder pallets.

Rule:
- Thicker walls = longer pallet life (greater number of wave solder cycles).
- Thinner walls = lower pallet life (lower number of wave solder cycles).

0.125 inch clearance violations that lead to pallet wall thickness of 0.025 inch will yield extremely short pallet life. If a design cannot yield to these requirements and must survive many thermal excursions, individual pockets (of the wave pallet) can be fitted with titanium inserts. These inserts are very expensive and can increase the cost of a pallet by 30-50% or higher (depending on the number of titanium pockets required per pallet).

The height of SMD components on the backside should not exceed .090". There can be some isolated areas that can exceed this to a maximum height of .120". The cavity in the fixture will be modified in these areas and should not affect the life of the fixture. All parts that exceed these criteria will most likely be hand soldered.

Orientation of the SMD components is not critical in this process.
7.0 Pad Configuration

7.1 Fine Pitch Components (Pitch ≤ to .025")

The length of the pad should extend .020" away from the toe and heel of the lead itself. The width should be 50-55% of the pitch. These should be non-solder masked defined pads.
7.1 Fine Pitch Components (Pitch ≤ to .025”, CONTINUED)

Local fiducial should be positioned in each fine pitch location to improve the placement accuracy of the device. Single fiducial pattern must have fiducial centered within device footprint. Dual fiducial pattern must locate fiducials equally spaced from footprint center (mirror image along both diagonals).

Figure 20: Fine pitch land pattern recommendations.
7.2 BGA Components

BGA Pad sizes are dependent on the pitch of the components. The pad geometry should be as follows:

![Local Fiducial architecture](image)

**Figure 21: Local Fiducial architecture.**

<table>
<thead>
<tr>
<th>Package Type</th>
<th>PCB Pad Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBGA</td>
<td>.0285&quot; +/- .0015&quot;</td>
</tr>
<tr>
<td>1.5 mm pitch PBGA</td>
<td>.025&quot; +/- .001&quot;</td>
</tr>
<tr>
<td>1.27 mm pitch PBGA</td>
<td>.023&quot; +/- .001&quot;</td>
</tr>
<tr>
<td>1.0 mm pitch PBGA</td>
<td>.020&quot; +/- .001&quot;</td>
</tr>
</tbody>
</table>
The traces that connect vias to BGA pads need to be masked off as a minimum to prevent solder from scavenging into the vias. The BGA pads are non-solder masked defined.

![Diagram of a BGA pad with a via and a non-solder masked area defined.]

**Figure 22: Masked via on BGA pad.**
8.0 Surface Mount/Wave Solder Tooling and Stencil Fabrication

Guideline
CAD data is the preferred format of data exchange.
The following are the preferred standard CAD data formats used for the design of fixtures and tooling:

- Gerber
  - Basic or Standard Gerber (RS274D) – requires a separate aperture file
  - Extended Gerber (RS274X) – embedded aperture data
- ODB++
  - ODB++ is an intelligent format that captures all the CAD/EDA, assembly and PCB fabrication knowledge in one single database. This format takes the place of individual gerber, drill, and aperture files, and adds additional information that helps produce more accurate, higher quality fixtures.
- FTP (File Transfer Protocol) is the preferred data transfer method over email when data package exceeds 5 MB of file size. Please contact Vanguard for FTP access information.

8.1 Data Requirements:
2. Global fiducials must be incorporated in the paste files.
3. Read me files describing what the Gerber files are.
4. A drawing of the board in AUTOCAD .DWG, .DXF or PDF format is desirable. A drawing in Gerber or HPGL format are also acceptable.
5. A sample board is desirable.
6. If the boards are multiple imaged on a panel (flat), a step and repeat drawing of the panel layout or GERBER data for the panelization is required. We would desire this in the same .DWG or .DXF format. A hard copy drawing is an acceptable alternative.

8.2 Stencil Data requirements:
1. Paste, Silkscreen and Mask layer. If PCB is two sided, data is needed for each side.
2. Silkscreen layer(s) should include reference designators, polarity markings and part outline. Refer to Section 5.4 for more details.
3. PCB outline.
4. Fiducials
5. If more than one image, panelized paste layer(s) and overall PCB layout showing entire PCB with image outlines.
6. Special customer requirements for apertures.

8.3 Tooling Data Requirements:
1. PCB Fabrication Drawing: Gerber, pdf, .dwg, .dxf are acceptable formats
2. Solder mask, Silkscreen, and Paste Gerber layers. Top and bottom as applicable.

9.0 CAD Data Requirements for Placement Programming

9.1 CAD File
A. Ascii Cad: Many Cad/PCB Board Design Software application allow for the export of Cad data in ASCII (text) format. This data can be imported directly into Unicam or Fabmaster at Vanguard to generate SMT machine programs and test programs, respectively.
B. The following are extraction procedure and typical header output of the more popular PCB Design Software. Vanguard can provide instructions for exporting ASCII CAD specific to a CAD/PCB Design Software application.:

- Cadence Allegro
- Extraction Procedure:
Cadence Allegro requires the use of a script available from www.aiscorp.com. The script produces a "ccam.cad" file that can then be imported into CircuitCAM.

Common File Extension: ".cad"

File header:

cam

102.brd!Tue Apr 25 15:21:27 2000!-100.000!-940.000!430.000!0.001!millimeters!B01!47.2

A Cadence Allegro file can be very easily distinguished by the !marks in the output file.

29 data fields are required in the output file.

- GenCAD v1.4 from Veribest

Extraction Procedure:
Veribest provides a stand-alone application called Report Writer. Use this application to export the "Mitron" export option, which causes Veribest to produce a GenCAD compliant output ASCII file.

Common File Extension: ".cad"

File Header:
$HEADER
GENCAD 1.4
USER RSI-TRANSLATOR GENCAD OUTPUT V:10
DRAWING scm
UNITS USER 1000
ORIGIN 0 0
INTERTRACK 0
$ENDHEADER

9.2 BOM file

A. File format: Soft copy in ASCII or plain text, comma delimited or tabular. Columnized, Excel format preferred.

B. Description: This file SHOULD provide accurate information on:

1. Customer part numbers.
2. Part Description, which contains the identification of the component itself. This aids in validating that the correct components are issued to the floor. Include part type in description: CBGA, PBGA, SOIC8, etc.
3. Reference Designators.
4. Qty per part number.
5. BOM Notes, which highlight any instructions regarding the part number.
6. Separate DNI (Do Not Install) list. SMT Components identified as "DNI" will not have apertures cut in the solder stencil.
7. See Table 21 for an example of the preferred BOM structure.

<table>
<thead>
<tr>
<th>Item Number</th>
<th>Part Description</th>
<th>Ref Des</th>
<th>Qty</th>
<th>BOM Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000016-001</td>
<td>IC 74HC00 QUAD 2 INP</td>
<td>U108,U128,U138,U158</td>
<td>4</td>
<td>No Clean Only</td>
</tr>
<tr>
<td>1000039-001</td>
<td>IC, 74HC245 OCTGAL XCVR</td>
<td>U23A,U23B</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

Table 22 Example of Preferred BOM Structure

1. SILKSCREEN GERBER files (Top and/or Bottom)
Design for Manufacturability Manual

Type: Work Instruction
ISO Section: 2.0-27

Document # 11566-021
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A. File Format: CAD output in either Gerber or HPGL formats.
B. Description: This file is required if the assembly drawing (hard copy) or board PCB is not readily available.
C. Required for: Pick and place program generation, Vanguard EMS process for templates, work instructions, procedures and documentation.

2. AVL
A. File format: Hard copy or ASCII file acceptable.
B. Description: Should list all acceptable manufacturing part numbers for each device location.
C. Required for: Verification of placement, and work instructions throughout the process.

5. Panel Drawings (Refer to Section 3.3 for more details)
A. Total X and Y dimensions of PCB
B. Fiducial locations defined.
C. Distance from PCB corner to first image.
D. Distance between images.

10.0 Mechanical Requirements for PCBAs

10.1 Torque Requirements for Hardware

The assembly drawings or assembly instructions should specify the torque requirements for all hardware attached to the PCBA. Examples of hardware needing torque requirements are shown below:

1. Screws for sheet metal
2. Component hold down screws
3. Standoffs
4. Connector hardware and hold down screws
5. Fittings for pneumatic components

Table 23 lists the possible torque values for various types and sizes of screws. It is the customer’s responsibility to evaluate these values and ensure they are proper for the environmental conditions that the assembly is designed for.

10.2 Self-Clinching Fasteners

The PCB layout should provide a minimum of 3mm clearance order to have sufficient clearance for tooling used for inserting the Self-Clinching Fastener. In cases where the manufacturer recommends a larger clearance than 3mm, then the manufacturer’s recommendation should be followed.

The pad design for the Self-Clinching Fastener should be per the manufacturer’s recommendations including hole size, plating requirements and recommended application.

10.3 Press Fit Connectors

The PCB layout provides sufficient clearance on the top and bottom side of the PCBA for access for the press fit tooling per the manufacturer’s recommendation. Designs with components placed too close to the press fit connector may require special tooling and fixtures to for proper insertion of the connector.

PCBAs that are thinner than 0.061” will require a base fixture to prevent damaging the board and surrounding components during the press operations.

11.0 System Integration (box build)

11.1 Cosmetic Specifications

Cosmetic specifications should be provided detailing the criteria of inspection for cosmetic blemishes. The specification should outline the magnification used for inspection, the distance and angle used for inspection.
11.2 **Fabricated parts**  
Drawings should be supplied for all fabricated components. Drawing should include specific information on material, tolerance and finish requirements.

11.3 **Assembly Drawings and Work Instructions**  
Assembly drawings and work instructions should be provided, defining the sequence of the assembly process. Critical aspects related to the building of the product as well as torque specifications for any hardware should be defined. Complex assemblies should have drawings broken into sub-assemblies or the specific build sequence. In the absence of torque specifications Vanguard will default to ASME standard torque table.

11.4 **Packaging**  
Instructions should be supplied illustrating the packaging requirements for the product. These instructions should include all label requirements, foam inserts, literature, box and bag requirements.

Labels, literature and packaging materials should be on the BOM.

In the absence of shipping instructions and customized packaging, Vanguard will default to the following:

1) Supply parts free from all contamination
2) When items are ESD-sensitive, packaging will be ESD safe and labeled appropriately
3) Ship in packaging that ensures adequate protection from mechanical/ESD damage during ordinary handling and shipping.
4) Packaging shall meet the minimum packaging requirement of the common carriers.
## Appendix A – Critical Item DFM Checklist

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Critical Items for Pre-DFM Consideration</th>
<th>DFM Manual Section</th>
<th>Options</th>
</tr>
</thead>
</table>
| 1        | Documentation Requirements: CAD Data Requirements for Placement Programming, BOM format, PCB Spec Dwg (initial review by tech support) | 9                  | 1. Request data from customer  
2. Produce centroid files from GERBER                                    |
| 2        | Board Dimensions: Length, Width, Thickness. Will this fit into a standard process? (max 18x16x0.062)     | 4                  | 1. No bid  
2. Hand solder  
3. Outsource build  
4. Special tooling to run on SMT                                          |
| 3        | Fiducials: Size, Features and Locations. Are fiducials present? Correct size / features? Right locations? This includes arrays if the customer is providing the array data | 3.6 3.3.1           | 1. Request customer to add  
2. Vanguard add panel rails/frame to add fiducials  
3. Use alternate features if available  
4. No bid                                                               |
| 4        | Manufacturability vs. Form factor (shape). Irregular shape, too small for machine? Panelization or fixtures required? | 4.7                | 1. Create panelization layout  
2. Use SMT fixtures                                                        |
| 5        | Tooling holes - method for securing boards. This includes arrays if the customer is providing the array data | 4.2 3.3.1           | 1. Request customer to add holes per DFM manual.  
2. Vanguard add panel to add tooling holes  
3. Use edge clamps                                                       |
| 6        | SMD Size Requirements and Capabilities. Are these components within our placement capabilities? SMT heights proper for Selective Wave solder? | 5.4                | 1. Hand solder, specify # of leads  
2. Place using SRT  
3. Place in paste  
4. DNI  
5. Use Special tooling                                                    |
| 7        | Component Spacing. SMT to SMT spacing. Spacing around BGAs. Can a standard process be used?             | 5.2                | 1. Machine place  
2. Hand place in paste  
3. Hand solder, specify # of leads                                      |
| 8        | Plating Recommendations. Is plating appropriate for the assembly technology?                           | 3.2                | 1. Recommend different plating  
2. Run as is                                                              |
| 9        | Double Sided Assemblies for Wave Solder. Th-to-SMT spacing for standard process?                        | 6                  | 1. Hand solder, specify # of leads  
2. Titanium Wave Fixtures                                                 |
| 10       | De-panel / Tab Routing Guidelines. Can we de-panel this? V-score or mouse bite. Parts too close to de-panel features. | 4.3                | 1. Request customer change type &/or placement of de-panel design  
2. Hand solder parts close to de-tab  
3. Use dremel tool to de-tab                                               |
| 11       | Component spacing around PEMs. PEM diameter +3mm (minimum) spacing.                                      | 10.2               | 1. Recommend customer change spacing  
2. Component to be hand soldered  
3. Custom tool required.                                                   |