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Vanguard EMS Inc.
3725 S.W. Hocken Ave.
Beaverton, OR 97005

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<th>Title</th>
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1.0 Documentation Definition

1.1 Purpose
The purpose of this document is to provide design and circuit board layout information that will help maximize manufacturability and yields of circuit boards at Vanguard EMS, Inc. This document will aid our customers in understanding Vanguard EMS assembly, test processes and manufacturing equipment requirements. This will help reduce product introduction times and reduce total manufacturing costs.

1.2 Scope
This design guide is intended to supplement, not replace existing design standards. The information presented herein is based, in general, on IPC-7351A.

As a minimum, Vanguard EMS will perform a “Critical Item” Design for Manufacturing review for all quotes and first time builds. These Critical Items are defined in Appendix A. Appendix A also identifies potential options to resolve a violation of these “Critical Items”.

If requested by the customer or at the discretion of Vanguard EMS, a complete DFM review will be performed on an assembly, especially if the design is complex or of critical nature and provide a detailed DFM Report.

1.3 Controls
This document is internally controlled at Vanguard EMS and will need to be verified as to current level.

1.4 PCB Array Specific Requirements

3.3.1 – Required Array / PCB Features
3.3.2 – Recommended Array Design
3.6 – Fiducial Requirements
4.2 – Tooling hole requirements
4.3 – De-Paneling/Tab Routing Guidelines
4.4 V-Score Array Dimension Considerations

2.0 Board Architecture

2.1 Guidelines for Using/Designing Through-Hole and SMT
Ideally boards should be 100% SMT or 100% through-hole. Boards that use both technologies are referred to as Hybrids. The usage of through-hole parts should be minimized as much as possible. Boards that require at least two separate processes to manufacture inherently add both manufacturing time and cost. When through hole components are required Vanguard will hand install. Soldering can be accomplished via wave/selective solder or by hand.

3.0 PCB Construction and Design

3.1 Bow and Twist
The maximum allowable bow and twist for SMT application is 0.75%, not to exceed .090”. The maximum allowable bow and twist for pure through-hole component designed PCB’s is 1%.
### 3.2 Plating Recommendations

The following matrix (Table 1) defines what plating finishes are best suited when specific component packages are used. They are defined by preference (1 being best).

<table>
<thead>
<tr>
<th>Condition</th>
<th>Assembly Type</th>
<th>Specific Component Technology Used</th>
<th>OSP Note 1</th>
<th>IM/SN</th>
<th>ENIG</th>
<th>IM/AG</th>
<th>HASL</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100% SMT:</td>
<td>BGA, CSP, Fine Pitch: 16-49 Mil.</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>1</td>
<td>N/A</td>
<td>BGA, CSP requires flat planar mounting surfaces.</td>
</tr>
<tr>
<td>2</td>
<td>100% SMT:</td>
<td>No BGA, NO CSP, Coarse Pitch Greater than 50 Mil.</td>
<td>4</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>Coarse pitch compatible with HASL.</td>
</tr>
<tr>
<td>3</td>
<td>Hybrid SMT + Through Hole:</td>
<td>BGA, CSP, Fine Pitch 12-49 Mil Pitch</td>
<td>3</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>N/A</td>
<td>BGA, CSP requires flat planar mounting surfaces.</td>
</tr>
<tr>
<td>4</td>
<td>Hybrid SMT + Through Hole:</td>
<td>No BGA, NO CSP, Coarse Pitch Greater than 50 Mil</td>
<td>4</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>Coarse pitch compatible with HASL.</td>
</tr>
<tr>
<td>5</td>
<td>100% Through Hole</td>
<td></td>
<td>4</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>Coarse pitch compatible with HASL.</td>
</tr>
<tr>
<td>6</td>
<td>100% Press-Fit</td>
<td></td>
<td>4</td>
<td>5</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>HASL = ideal finish</td>
</tr>
<tr>
<td>7</td>
<td>Hybrid Press-Fit</td>
<td>BGA, CSP, Fine Pitch 12-49 Mil Pitch</td>
<td>3</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>N/A</td>
<td>HASL not acceptable. Insertion lube required.</td>
</tr>
<tr>
<td>8</td>
<td>Hybrid Press-Fit</td>
<td>No BGA or CSP, Coarse Pitch Greater than 50 Mil</td>
<td>4</td>
<td>5</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>HASL requires no insertion lube. All other use lube</td>
</tr>
<tr>
<td>9</td>
<td>Lead Free Solder Requirements</td>
<td>ALL SMT Technologies, WITH OR WITHOUT THROUGH HOLE, INCLUDING PRESS-FIT</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>N/A</td>
<td>LEAD FREE WITHOUT PRESS-FIT</td>
</tr>
<tr>
<td>10</td>
<td>Lead Free Solder Requirements</td>
<td>ALL SMT Technologies, WITH OR WITHOUT THROUGH HOLE, INCLUDING PRESS-FIT</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>N/A</td>
<td>LEAD FREE WITH PRESS-FIT</td>
</tr>
</tbody>
</table>

**Table 1: PCB Plating Recommendations**

- OSP: Organic Solderability Preservative, ENIG: Electroless Nickel Immersion Gold
- Im/Ag: Immersion Gold, Im/Sn: Immersion Tin, HASL: Hot Air Solder Level

**Note 1:** OSP must allow for solder deposit on all test points to meet minimum ATE probe-ability requirements.

**Note 2:** Solder deposit on OSP via must allow for no less than 8 mil gap between adjacent via’s. This will reduce solder bridging potential.

**Note 3:** For all Press-Fit applications consult connector manufacturer for finished hole size requirements and/or application requirements.
3.3 Board Construction and Fabrication

Thickness of surface mount boards should be a minimum of 0.031". Boards thinner than 0.062" may require SMT fixtures.

**Guideline**

All components **SHOULD** be marked with a reference designator and polarity indicator (Cathode or Bi-Directional indicators should be used for diodes; Pin 1 indicators should be present for filters), if applicable, on the silkscreen. The polarity indicator **SHALL** be visible after part installation. Table 2 shows the recommended reference designator location and polarity markings that should be incorporated in the silkscreen.

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>IDEAL CONDITION</th>
<th>ACCEPTABLE CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Component</td>
<td>Silkscreen (line) denotes location of chip (pad pairs). (exclude line for 0402 or smaller components.) Designators clearly identify location. Maximum tolerance allowable with silkscreen registration. Increase font on 0402, 0201 devices where possible.</td>
<td>Keep silkscreen off pads to prevent interference with paste inspection systems. Exclude silkscreen outline for 0402 or smaller components. Increased artwork complexity. No significant gains for manufacturing. Silkscreen generally has a generous alignment tolerance. Account for this when designing silkscreen outline to avoid overlap onto pad features.</td>
<td>(No designators, missing designators) Confusion to chip location (which pads belong to which chip) Cannot determine designators without documentation (BOM, drawings etc.) This condition will increase inspection cost and increase potential for wrong component loading.</td>
</tr>
</tbody>
</table>
### Orientation and Reference Designators

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>IDEAL CONDITION</th>
<th>ACCEPTABLE CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>R500</td>
<td>R501</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>R502</td>
</tr>
<tr>
<td>Orientation and Reference Designators</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Text orientation follows device orientation.

| Orientation and Reference Designators (cont.) |           | R501 | R503 | R504 |
|                                             |           |      |      |      |
| Text clearly separated from adjacent devices. |           |      |      |      |
| Nomenclature is consistent.                  |           |      |      |      |
| Text orientation follows device orientation. |           |      |      |      |
| Avoid confusing reference designator orientation and alignment. | |      |      |      |

Avoid silkscreen reference designators on via features. Small (0603 and smaller) will become difficult (or impossible) to read when silkscreen is printed on via.
Polarized Capacitors

Mark the Anode (+) side of the capacitor silkscreen.
Use a bar or line equal to the width of the pad. This is a “polarity indicator”. The component (generally) will have a matching line.
Ideal polarity indicators have a mark on the board that matches the mark on the part. Though impractical for all device types, there is excellent consistency on polarized capacitors.

Mark the Anode (+) side of the capacitor.
The (+) or (dot), though adequate for indicating polarity, they don’t match the (general) standards of SMT polarized capacitors (which use lines or bars).

Unmarked polarized locations increase the complexity of the assembly process. These add delays for first article processes and can even be dangerous if polarized capacitors are mounted reversed.
Components do not (generally) have a matching “A”. These marks (or lack of) will increase manufacturing costs and delays.

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>IDEAL CONDITION</th>
<th>ACCEPTABLE CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diodes (including LEDs)</td>
<td>![Diode Symbol]</td>
<td>![Diode Symbol]</td>
<td>![Diode Symbol]</td>
</tr>
<tr>
<td>Uni-directional</td>
<td>Bi-directional</td>
<td>Anode (A) and Cathode (C or K) or the diode symbols are the only clear orientation indicators for diodes (including LEDs). These symbols remove all ambiguity from the process. Bi-directional symbols are ideal when the diode does not have polarity.</td>
<td>Dots or lines identify the Cathode end. Some designers use these symbols to identify the anode and others use the same symbols to indicate the cathode. Even a plus sign is sometimes used as an orientation mark for the cathode. Therefore, this marking method is not acceptable.</td>
</tr>
</tbody>
</table>

The highest reliability for mounting components in the correct orientation is to “match alignment marks” (part polarity identification to silkscreen mark).

Component IDEAL CONDITION

Acceptable Condition

Poor Condition

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<table>
<thead>
<tr>
<th>Component</th>
<th>Design Feature</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOIC SOP, SSOP etc.</td>
<td>Notice how the &quot;notch&quot; is exaggerated away from the device allowing for simple inspection after placement.</td>
<td>Mark should be clearly visible when component is mounted.</td>
</tr>
<tr>
<td>QFP, TQFP</td>
<td>Polarities mark is large and easily found.</td>
<td>1 Polarity mark is not easily recognizable.</td>
</tr>
<tr>
<td>BGA</td>
<td>Silkscreen outline should be slightly larger than BGA device.</td>
<td>Poor design. Atypical method is not easily recognizable.</td>
</tr>
</tbody>
</table>

Table 2: Component silkscreen and orientation table.
Guideline
SMT components should be located (no closer than) 0.300 inch from the edge of the PCB. Violation of these (keep-out) clearance requirements will require the addition of edge rails to the PCB or custom fixtures (3.3.1).

3.3.1 Required Array / PCB features
- PCBs exhibiting any violation of component keep-out regions may require break-away rails on all sides.
- Break-away rails (including .100” route channels) should measure 0.400” unless specified by Vanguard Engineering.
- Image PCB’s will be centered in array frame on both axes.
- Fiducials shall be added to each array frame in accordance with section 3.6. Fiducials shall be 0.039” ±0.010”. Image fiducials should also be added within the array frame whenever possible.
- Fiducials shall not reside within 0.125” of card edge or array frame edge.
- Array designs shall have 0.125” +0.002” un-plated tooling holes positioned 0.200” up from the bottom of the array perimeter and 0.500” down from perimeter’s top edge. All tooling array tooling holes should be positioned 0.200” in from the sides. See Figure 2 for example.
An array design drawing should be provided to Vanguard to allow for accurate stencil design and Pick-and-Place programming. The array drawing should provide the following information:

- Array dimensions length and width.
- Break-away rail dimensions.
- Step-and-repeat dimensions.
- Fiducial locations.
- Tooling hole locations.
- Routed section callouts.
- Jump score callouts.
- Image numbers.
- See Figure 3 for example.
3.3.2 Recommended array design: V-score option in left column; tab option in right column (solid tab and mouse-bite). See Figure 4 for example.

Figure 5: Array design requirements.

Figure 4: Array design.
3.4 Micro Via / Via-in-pad

If via-in-pad is required in the design, then, as a minimum, the via-in-pad should be copper capped. Additionally, the opposite side of the via should either be:
- Copper capped if used as a test point for ICT
- Masked or filled over to prevent entrapment of plating chemicals.

If via-in-pads are not capped, the following conditions could result adding additional assembly cost:
- Solder wicking to opposite side causing paste printing issues on second pass (if via-in-pad is on the first pass side) which may result in solder bridging and solder balls
- Solder scavenging resulting in insufficient solder and voids in BGA solder balls

3.4.1 Standard Via

Clearances
Standard Via’s need to maintain minimum clearances from adjacent conductors. These clearances are a function of via type (masked or exposed). Masked vias require less clearance. Exposed vias require greater clearances to adjacent exposed conductors.

3.4.2 Via Size Guideline

Table 3 lists the recommended Via size guidelines. For Type II attach methods there must be a .025" diameter area free of vias at the centroid of each passive device on the secondary side as shown in Figure 5. Vias placed in this region “rob” adhesive, which makes it difficult to bond the device to the board for wave solder. This design rule is only valid on Type II designs that use epoxy attach methods for wave solder immersion.

<table>
<thead>
<tr>
<th>Via Type</th>
<th>Outside Ring Diameter</th>
<th>Hole Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>.030&quot;</td>
<td>.020&quot;</td>
</tr>
<tr>
<td>Alternative</td>
<td>.020&quot;</td>
<td>.013&quot;</td>
</tr>
<tr>
<td>Alternative</td>
<td>.019&quot;</td>
<td>.011&quot;</td>
</tr>
<tr>
<td>Test Point</td>
<td>.035&quot;</td>
<td>.020&quot;</td>
</tr>
</tbody>
</table>

Table 3: Via Size Guideline

Figure 5: Epoxy keep-out region (type II attach method).

3.4.3 Masked Vias

Masked vias are preferred. This method should be employed as a default design method. Masked vias offer the greatest resistance to solder bridges or shorts.
3.4.4 Exposed Vias

Exposed vias are not covered in solder resist (mask). These are exposed conductors which, in certain circumstances, can allow solder shorts to occur. Clearances for exposed vias are dictated by adjacent artwork features.

![Exposed via / masked via graphic.](image)

3.4.5 Rules for Masking Vias under BGAs

It is Preferred that BGA via’s be masked as a default design rule.

Masked vias are the best method to prevent solder shorts under BGA’s.

Chip Components

Chip components can shift or skew during the reflow process. This can cause the component termination to short across to adjacent exposed conductors (vias). Therefore, the via “keep-out” spacing is dictated by the component termination width. See Figure 7 from good design practices for vias associated with chip components.

Exposed Via Location Rule: Adjacent to SMT pads. Exposed vias should be a minimum of 50% component termination width + 0.020 inch. This will ensure chip component shift / skew will not create a solder short.

Exposed Via Location Rule: End of SMT pads. Minimum clearance 0.020 inch from exposed conductors.
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Figure 7: Pad Isolation techniques

<table>
<thead>
<tr>
<th>Example</th>
<th>POOR DESIGN</th>
<th>ACCEPTABLE DESIGN</th>
<th>PREFERRED DESIGN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SMT PAD &lt;--- SHORT CIRCUIT --- UN-MASKED VIA</td>
<td>SMT PAD &lt;--- SHORT CIRCUIT &lt;--- A &gt; B</td>
<td>SMT PAD &lt;--- SHORT CIRCUIT --- UN-MASKED VIA</td>
</tr>
<tr>
<td></td>
<td>Shifted Resistor. Meets IPC-610, class 1,2,3 for alignment. However, resistor is shorted to adjacent via. May not meet minimum electrical clearances. Not Acceptable</td>
<td>'A' is greater than 'B'</td>
<td>End Clearance: Via is not Maintain a minimum conductor clearance of 0.020 (as measured from via annular ring to adjacent conductors).</td>
</tr>
<tr>
<td></td>
<td>SMT PAD &lt;--- SHORT CIRCUIT --- UN-MASKED VIA</td>
<td>SMT PAD &lt;--- SHORT CIRCUIT &lt;--- A &gt; B</td>
<td>SMT PAD &lt;--- SHORT CIRCUIT --- UN-MASKED VIA</td>
</tr>
<tr>
<td></td>
<td>Skew resistor causing short to via. Passes IPC-610 for alignment (class 2,3). Not Acceptable</td>
<td>Via enters chip keep out area. Acceptable</td>
<td>End clearance: Maintain a minimum conductor clearance of 0.020 (as measured from via annular ring to adjacent conductors).</td>
</tr>
</tbody>
</table>

Table 4: Exposed via locations.

3.5 Runs & Ground Planes

Guideline

All ground/power planes should be internal to the board and located symmetrically about the center of the thickness. This will minimize the board from warping.

Guideline

All traces should be as equally distributed as possible in both the X and Y directions and should not be oriented in only a single direction on each layer. This will minimize the board from warping.
3.6 Fiducial Requirements

Fiducials are required for manufacturability, and fiducial registration is the primary SMT manufacturing registration method.

It is recommended that the Fiducials conform to the illustrations shown in Table 5. Fiducial target diameter may range in size ±0.010". Deviation from this requirement could prevent the SMT vision system from properly aligning the PCB.

Solder mask isolation is required. Omission of this feature will reduce the accuracy of Vanguard’s SMT placement equipment and increase delays. Holes or land patterns should never be considered as registration marks. Land patterns are often covered with solder paste and rendered unusable to the SMT vision system. Through-holes or vias are poor choices (as fiducials) due to the fact that drill wander causing hole tolerances that are significantly greater than lithographic etch processes used for copper artwork. Fiducials are purpose-built artwork features and are mandatory to standard manufacturing strategies.

Table 5: Fiducial Design

Fiducials should be located, non-symmetrically, in three corners of each image and in three corners of the array. Fiducials should be located as far apart as possible and should be in the same plane on each axis.
3.7 Polyimide flex and rigid flex assemblies

Flex assemblies introduce another variable to manufacturing. The flexible nature of the Polyimide coupled with its minimal thickness will require a supporting fixture through the SMT manufacturing process. Rigid flex assemblies, depending on configuration, may require special considerations. These special considerations often are design dependent.

Recommendations:

1. Fiducial features are required.
2. Keep all SMT to a single side.
3. Tooling holes (locating holes) cannot be used on materials thinner than 0.031 inch. The tooling pins interfere with the solder printing process.
4. No-clean process is preferred. Type I or Type II assembly should employ no-clean flux. Water soluble process will require a bake-out process between the first SMT pass and the second SMT pass. This is to prevent de-lamination but adds significant delays to the assembly process.
5. Polyimide is extremely hydroscopic and is dimensionally unstable. Typical growth is 1 - 3%. This undesirable attribute will affect mounting accuracies.
   a. Restrict passive components to no smaller than 0603.
   b. Active (I.C’s) to greater than 0.65mm pitch
   c. Devices with pitch smaller than 0.65mm must use a local fiducial.
6. Do not select snap-in devices for use with flex assemblies (Example: RJ45 connectors, Mictor staked connectors etc.)
7. Snap-in or staked devices are acceptable for rigid assemblies. However, if a double sided SMT attach is required, the stakes must not protrude.
8. Overhanging devices on rigid only assemblies should employ strain relief. Use of (integrated) solder tabs or adhesive (attachment) is preferred. Failure to utilize strain relief can result in lifted solder lands.

Figure 8: Fiducial location strategy.
9. Use of flex assembly arrays should employ minimalist strategies. Larger is not necessarily better with flex assemblies. Arrays are design specific. Consult with Vanguard Engineering.
10. Rigid flex assemblies should consider a built-in strain relief when using buried flex layer or when Polyimide is less than 0.010 inch. This is to prevent a “fold” or shear point, which will crack the copper conductors.
11. Flex/Rigid flex assemblies should consider purpose-built packaging to prevent folding of the Polyimide and subsequent component damage.
12. With rigid/flex designs, a minimum of 0.3 inches (prefer 0.4 inches) between board images. This is needed for the fabrication vendor to manually adjust the flex material prior to press. This spacing will also depend on the design.
13. With rigid/flex designs, tabs are the preferred method of keeping the image attached to array. V-score is possible but it will mean an extra step either at the fabrication or manufacturing process to cut the flex material.

4.0 Dimensional Considerations

4.1 Maximum Board profile with Components

The board size Vanguard EMS is capable of processing is dictated by the types of processes required to assemble the PCB. (ALL UNITS IN INCHES)

<table>
<thead>
<tr>
<th>PROCESS</th>
<th>MINIMUM SIZE</th>
<th>MAXIMUM SIZE</th>
<th>THICKNESS (MIN.)</th>
<th>THICKNESS (MAX.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMT</td>
<td>2 X 3.75</td>
<td>18 X 16&quot;</td>
<td>0.010</td>
<td>0.196&quot;</td>
</tr>
<tr>
<td>AOI</td>
<td>2 X 3.75</td>
<td>23.6 X 23.6</td>
<td>0.010</td>
<td>0.196&quot;</td>
</tr>
<tr>
<td>AQUEOUS WASH (WITH BASKET)</td>
<td>NONE</td>
<td>19-1/8 X 19-1/8</td>
<td>NONE</td>
<td>2-1/16</td>
</tr>
<tr>
<td>AQUEOUS WASH (NO BASKET)</td>
<td>5 X 5</td>
<td>23 INCH WIDTH</td>
<td>0.010</td>
<td>2.5</td>
</tr>
<tr>
<td>OA WAVE SOLDER</td>
<td>2 X 2</td>
<td>17 X 20</td>
<td>0.031</td>
<td>0.196&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 INCH ABOVE BOARD CLEARANCE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NO-CLEAN WAVE SOLDER</td>
<td>2 X 2</td>
<td>15 X 18</td>
<td>0.031</td>
<td>0.196&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 INCH ABOVE BOARD CLEARANCE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LEAD FREE, NO-CLEAN WAVE SOLDER</td>
<td>2 X 2</td>
<td>15 X 18</td>
<td>0.031</td>
<td>0.093</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 INCH ABOVE BOARD CLEARANCE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PRESS-FIT</td>
<td>2 X 2</td>
<td>24 X 48</td>
<td>0.062</td>
<td>0.3937</td>
</tr>
</tbody>
</table>

1 Larger sizes are available for small prototype batch production. Contact Vanguard directly for specifications.
2 PCB thickness has a +/- tolerance. Maximum thickness must not be exceeded.

Table 6: Board size capabilities.

4.2 PCB Tooling Holes

Two tooling holes per PCB are needed for registration of board for JCT test. Recommended hole sizes are 0.125 ±0.002". Tooling holes should be un-plated. The area over the tooling holes should be free of mechanical interference to a height of 1" inch. The positional tolerance from tooling hole to tooling hole, center to center, should be +0.004" / - 0.000". Tooling holes should be placed 0.200" x 0.200" (same axis) from the bottom corners and 0.200" in and 0.500" down from the top corners of the PCB.

4.3 De-panneling/Tab Routing Guidelines

Board assemblies can be de-tabbed at Vanguard EMS using perforated breakaway tabs, v-groove breakaway tabs or hand cutting with a de-tabbing tool. These guidelines will reduce board damage or
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scrap for the de-paneling process. Following these guidelines will help prevent damage to both components and the board during de-paneling and prevent flooding during the wave solder process.

All designs must have SMT components placed a minimum of 0.100” from the board edge. All other features (runs, vias, through hole components, etc.) must have a minimum of 0.050” clearance from the board edge. Tables 7 and 8 show the preferred PCBA design for SMT and through hole to PCB edge clearance for de-panelization, along with the manufacturing risk level when the recommended clearance is not maintained.

Break-away designs should have perforation holes that are typically spaced at 0.050” intervals. The location of the breakaway edge will affect the smoothness of the edges.

The slightly inset version is preferred because it will require the least amount of additional labor to clean up. Tabs are typically spaced 3” on center (not to exceed 4.0”). Place tabs approximately 1.00” from corners to reduce sagging during reflow or wave soldering. It is desirable to have at least one tab per side. Figure 9 shows Vanguard’s preferred break-away tab design.

<table>
<thead>
<tr>
<th>Component Clearance</th>
<th>Preferred</th>
<th>Acceptable</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.100”</td>
<td>0.070”</td>
<td>Less than 0.070”</td>
</tr>
<tr>
<td><strong>Conditional</strong></td>
<td>No tabs shall be within .750” along the route cut axis to the nearest SMT pad edge or component body.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Manufacturing Risk</th>
<th>Preferred</th>
<th>Acceptable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lowest</td>
<td>Higher</td>
<td>Highest</td>
</tr>
</tbody>
</table>

Table 7: Tab clearance.

<table>
<thead>
<tr>
<th>Component Clearance</th>
<th>Preferred</th>
<th>Acceptable</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.100”</td>
<td>0.050”</td>
<td>Less than 0.050”</td>
</tr>
<tr>
<td><strong>Conditional</strong></td>
<td>No tabs shall be within .750” along the route cut axis to the nearest SMT pad edge or component body.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Manufacturing Risk</th>
<th>Preferred</th>
<th>Acceptable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lowest</td>
<td>Higher</td>
<td>Highest</td>
</tr>
</tbody>
</table>

Table 8: V-score clearance.

Increasing component distances to break-away will reduce de-panel stresses on components. Clearances of less than 0.070 should only be used where ultra-miniaturization is required. On tab routed PCB’s, Hand placement and the hand soldering of these type of components after panel removal may be another option.

![Applicable for TAB and V-Score](image)

**Figure 9: Break-away design**

Edge Routing Guideline
Use .100” routed slots as a standard.

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Edge Rail Guideline
Parallel surfaces are required for a PCB to be processed in through an SMT line. This is to prevent skewing through the conveyor system. All odd shaped PCB’s MUST have edge rails incorporated to meet this requirement. Custom reflow fixtures would have to be developed if this requirement is not met. See Section 4.4 for recommendations.

4.4 V-score array dimensional considerations.
All V-score lines should follow the 1/3 rule illustrated in Figure 10.
Minimum thickness PCB = 0.032”
Maximum thickness PCB = 0.110”
Maximum V-score de-panel length = 18 inches

![Figure 10: V-score 1/3 rule diagram](image)

4.5 Component orientation and array break-away..
Figure 11: Component orientation vs. shear axis
4.6 Array design using V-score

The recommended array for v-score PCBAs is shown in Table 9.

<table>
<thead>
<tr>
<th>Ideal Condition</th>
<th>Poor Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low strength design. Susceptible to accidental breakage during manufacturing.</td>
<td>Cannot be de-panelled using standard equipment.</td>
</tr>
<tr>
<td>Vertical PCB rails use full score method. All others use jump score.</td>
<td>Not manufacturable using v-score.</td>
</tr>
<tr>
<td>Array frame offers good strength throughout the manufacturing process.</td>
<td>Not manufacturable using v-score.</td>
</tr>
</tbody>
</table>

**Table 9 Array design using v-score**

Uses standard depanel equipment.
### 4.7 Manufacturability vs. Form factor.

Table 9 shows the desired array to obtain the ideal manufacturability of a PCBA.

<table>
<thead>
<tr>
<th>PCB Condition</th>
<th>IDEAL CONDITION</th>
<th>ACCEPTABLE CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallels</td>
<td>All opposite sides are parallel.</td>
<td>Two opposite sides are parallel</td>
<td>No opposite sides are parallel</td>
</tr>
<tr>
<td>Keep-Out Violations</td>
<td>Any PCB that has ANY violation of component keep-out will utilize break-away rails on ALL sides.</td>
<td>See Ideal</td>
<td>See Ideal</td>
</tr>
</tbody>
</table>

#### Square

- **Key**
  - COMPONENT FREE
  - AVAILABLE COMPONENT REAL ESTATE

Keep out area on 4 sides offers maximum flexibility to the manufacturing process.

Parallel sides = ideal condition.

Require two pairs of parallel sides with no interruptions or voids along perimeter.

Easily stacked in card carriers.

<table>
<thead>
<tr>
<th>Condition</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SQUARE</td>
<td></td>
</tr>
</tbody>
</table>

Two parallel sides with component keep out.

Require two pairs of parallel sides with no interruptions or voids along perimeter.

Can be stacked in card carriers. However, components may come in contact with carrier. This carries a risk for component damage.

<table>
<thead>
<tr>
<th>Condition</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SQUARE</td>
<td></td>
</tr>
</tbody>
</table>

No component keep-out will require the use of break-away rails, full array frame or fixtures.

Fixturing condition = low manufacturability and increased cost.

Cannot be stacked in card carriers. Poor movement efficiency on factory floor.

<table>
<thead>
<tr>
<th>Condition</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SQUARE</td>
<td></td>
</tr>
</tbody>
</table>

#### Rectangle

<table>
<thead>
<tr>
<th>Condition</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RECTANGLE</td>
<td></td>
</tr>
</tbody>
</table>

Acceptable only if length to width aspect ratio is less than 1.4

#### Coupon fill regions and slots / voids

<table>
<thead>
<tr>
<th>Condition</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>COUPON FILL</td>
<td></td>
</tr>
</tbody>
</table>

All boards that are not "regular polygons" should utilize a full frame.

Board voids should be filled with a coupon if wider than 0.125 inch.

Slots or router (voids) should be no wider than 0.125 inch. There are no restrictions on length.

Following these recommendations allows for the maximum flexibility on the manufacturing line and will prevent equipment optical sensor malfunction and special equipment programming.

<table>
<thead>
<tr>
<th>Condition</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>COUPON FILL</td>
<td></td>
</tr>
</tbody>
</table>

No component, keep-out plus large PCB void will require the use of break-away rails, full array frame or fixtures.

<table>
<thead>
<tr>
<th>Condition</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>COUPON FILL</td>
<td></td>
</tr>
</tbody>
</table>
4.8 SMT Fixture Considerations

a. Figure 12 illustrates the SMT fixture design.

b. Fixtures including the board must not weight more than 2.0Kg. (4.4 lbs.)

c. SMT fixtures must use reflective surface on the underside (facing down) to allow for proper operation of IR optical sensors.

d. Fixtures will secure the array using tooling pins in all 4 corners. Tooling pins will correspond to tooling holes in the array and will be .200" in from the array sides. Tooling holes will be .500" down from the top of the array and .200" up from the bottom of the array.

e. Clearance perimeter by a minimum 1 inch. There may be situations where this is increased or decreased and is application specific.
4.9 Form Fit and Function Considerations
Form, Fit or Function conditions will default to IPC-A-610-D (which states): “Conditions that are not specified as defective or as a process indicator may be considered acceptable unless it can be established that the condition affects user defined form, fit or function.”

Any condition determined as non-compliant under Form, Fit or Function will have its requirements specified as “user defined” aka “customer requirements”. It is mandatory that these customer requirements are identified on: customer drawings, BOM, ECN, Temporary Deviations or specification sheets.

5.0 Component Placement, Spacing and Orientation

5.1 Termination
Only a single lead or termination should be placed on a land. Use Solder Mask Defined pads. Placing two or more lead terminations on a single land (See Figure 13), causes:
   a. Unpredictable solder flow.
   b. Component skewing
   c. Increased occurrences of “tombstoning” and “draw-bridging” defects.

Figure 12: Fixture clearance requirements.
5.2 Component Spacing

Definition: Spacing refers to the gap between adjacent conductors. Typical pad designs are larger than component terminations or leads. Therefore, the isolation required between conductors (pads) will be considered.

Tables 11a – 11c illustrates the recommended minimum spacing between various SMD components based on the SMT density.

NOTE:
*1 Standard Clearance = 250 mils. This clearance offers the greatest manufacturing flexibility possible. Co-planarity will determine if a step solder paste stencil is required. Refer to section 5.2.1 for exact clearance requirements.

*2 Reducing these clearances below 0.100 inch will increase complexity of any subsequent rework operations.

*3 RULE: Chip-to-Chip spacing rules.

![Component Spacing Diagram]

Figure 13: Shared land pattern.

<table>
<thead>
<tr>
<th>Manufacturable</th>
<th>Less Manufacturable</th>
<th>Difficult to Manufacture</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="chart.png" alt="Diagram" /></td>
<td><img src="chart.png" alt="Diagram" /></td>
<td><img src="chart.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

Table 11: Component spacing rules.

<table>
<thead>
<tr>
<th>Conventional Designs</th>
<th>CHIP</th>
<th>TANTALUM</th>
<th>SMALL OUTLINE</th>
<th>QFP</th>
<th>SOT23</th>
<th>PLCC</th>
<th>BGA</th>
<th>CSP</th>
<th>CBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP: Note 3</td>
<td>60</td>
<td>60</td>
<td>50</td>
<td>100</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>TANTALUM</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>50</td>
<td>100</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>SO</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>50</td>
<td>100</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>QFP / TSOP / VSOP</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>50</td>
<td>100</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>SOT23</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>100</td>
<td>100</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>PLCC</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>BGA</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>CSP</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>CBGA</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
</tbody>
</table>

Table 12c: Conventional Component spacing (dimensions are in mils)
High Density Designs

<table>
<thead>
<tr>
<th></th>
<th>CHIP</th>
<th>TANTALUM</th>
<th>SMALL OUTLINE</th>
<th>QFP</th>
<th>SOT23</th>
<th>PLCC</th>
<th>BGA</th>
<th>CSP</th>
<th>CBGA</th>
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</thead>
<tbody>
<tr>
<td>CHIP</td>
<td>50</td>
<td>50</td>
<td>40</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>TANTALUM</td>
<td>40</td>
<td>50</td>
<td>100</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>100</td>
<td>250</td>
</tr>
<tr>
<td>QFP / TSOP / VSOP</td>
<td>50</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>100</td>
<td>250</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>SOT23</th>
<th>50</th>
<th>75</th>
<th>50</th>
<th>75</th>
<th>75</th>
<th>50</th>
<th>100</th>
<th>250</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>CSP</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>CBGA</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td></td>
</tr>
</tbody>
</table>

Table 12b: High density component spacing (dimensions are in mils)

Ultra High Density Designs

<table>
<thead>
<tr>
<th></th>
<th>CHIP</th>
<th>TANTALUM</th>
<th>SMALL OUTLINE</th>
<th>QFP</th>
<th>SOT23</th>
<th>PLCC</th>
<th>BGA</th>
<th>CSP</th>
<th>CBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP</td>
<td>35</td>
<td>60</td>
<td>50</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>250</td>
</tr>
<tr>
<td>TANTALUM</td>
<td>25</td>
<td>40</td>
<td>25</td>
<td>50</td>
<td>50</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>250</td>
</tr>
<tr>
<td>QFP / TSOP / VSOP</td>
<td>30</td>
<td>75</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>250</td>
</tr>
<tr>
<td>SOT23</td>
<td>30</td>
<td>60</td>
<td>50</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>250</td>
</tr>
<tr>
<td>PLCC</td>
<td>30</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>250</td>
</tr>
<tr>
<td>BGA</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>250</td>
</tr>
<tr>
<td>CSP</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>250</td>
</tr>
<tr>
<td>CBGA</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
</tbody>
</table>

Table 12c: Ultra high density Component spacing (dimensions are in mils)

5.2.1 Component keep-out clearances vs. device co-planarity:

![Figure 14: Step stencil printing concept.](image)

Typical SMT stencil thickness is 5 mils. This encompasses standard device types of 0402, 0603 chip resistors/capacitors even 0.5mm fine pitch. However, if any device co-planarity exceeds the thickness of the stencil.
(which determines the height of the solder paste brick) then an open solder joint will be created. To combat this defect, it is possible to use step-stencil architecture. Step stencils are stencils that have specific regions that use thicker foil to create deeper solder deposits. For example, a standard 5 mil stencil foil can have a device type “stepped” up to 8 mils to allow for increased deposition of solder paste.

There are two methods we use for stepping stencils.

1. Lamination or additive process.
2. Etch away or subtractive process.

Both methods will yield the same results of selective deposition to combat co-planarity issues in components or increased solder volume requirements. Consequently, both step processes are applied in a “step facing down method”. This method prevents metal squeegee damage and offers the most accurate and repeatable printing method.

Typical devices that may require a step stencil are:

- Ceramic BGA (CBGA) devices that use high temperature balls (Pb90 / Sn10). Typical ball-to-ball co-planarity may range between 6 to 8 mils*.
- Pin Grid Array sockets or BGA adaptors. Rigid pin designs often have up to 10 mils* of co-planarity. Floating pin designs 5 to 8 mils*.
- How to calculate component Keep-out:
  1. Determine device co-planarity. Use ball-to-ball or lead-to-lead method.
  2. Select Column “Coplanarity is” for your co-planarity specification. Move down 1 row to the “Use” specification.
- See Table 13 for recommended keep out sizes

*Coplanarity is device specific. Consult manufacturers’ data sheet.

<table>
<thead>
<tr>
<th>Coplanarity is</th>
<th>Less Than 4.99 (mil)</th>
<th>Between 5.0 &amp; 7.0 (mil)</th>
<th>Greater Than 7.01 (mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use</td>
<td>NO LESS THAN 0.100 INCH COMPONENT KEEP-OUT (STANDARD + CONVENTIONAL DESIGNS)</td>
<td>USE NO LESS THAN 0.200 INCH COMPONENT KEEP-OUT</td>
<td>USE NO LESS THAN 0.250 COMPONENT KEEP-OUT</td>
</tr>
<tr>
<td>CORRECT</td>
<td>PGA</td>
<td>CBGA / PGA / ETC</td>
<td>CBGA / PGA / ETC</td>
</tr>
<tr>
<td>INCORRECT</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.3 Component Orientation
The geographic location of a component on a PCB can impact the manufacture ability of the board. The following are guidelines that should be considered for ease in assembly.

- BGA’s should only be placed on the topside of the PCB. This eliminates the possibility of open solder connections due to the weight of the part during second pass reflow. An added process step would be required to temporarily support the secondary side BGA’s during the second pass reflow process.

- BGA’s and larger QFP devices (> than 100 leads) should not be placed in the center of the PCB. The maximum board warpage tends to be in the center of the PCB. The result can be open solder connections. For a standard .062” PCB, this becomes a concern when the surface area exceeds 25 in².
If BGA’s are on both sides of the board, it is not recommended that the BGA’s are positioned on top of each other (See Table 14). This method makes rework of a BGA extremely difficult. In addition, this method makes x-ray inspection of the solder balls of the BGA very difficult.

<table>
<thead>
<tr>
<th>IDEAL CONDITION</th>
<th>POOR CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET MOUNT</td>
<td>MIRROR MOUNT</td>
</tr>
<tr>
<td>PCB SUBSTRATE</td>
<td>PCB SUBSTRATE</td>
</tr>
</tbody>
</table>

Simple x-ray inspection methods used. Simple rework methods used. Open architecture often advantageous for debug and testing. Very difficult x-ray inspection. Cannot easily fault-find. Rework of defective device may negatively affect mirrored device.

Table 14: BGA mounting strategy.

- All polarized surface mount or through-hole components should be placed in the same orientation and in only one axis. This facilitates ease in visual inspection.

5.3.1 Chip Under Device

Recommendations when employing chip under device:
- Chip under Dram or other device types can complicate inspectability, rework and device testing.
- Keep device thickness tolerance and process stack-up tolerances in mind when specifying chip under device.
- SMT solder has thickness. This dimension should be accounted for in the design. Typical device-to-pad gap is 2-3 mils.
- Devices placed under BGA sockets, chip carriers or ZIF sockets need to account for BGA ball collapse. Collapse is typically 20-30% of the ball diameter. However, the weight (density) of the ZIF and type of solder composition can affect the final clearance height. Keep stack-up tolerances in mind with these types of designs. This type of design practice is extremely risky due to:
  1. Inability for AOI or manual inspection of hidden devices.
  2. Extreme difficulty for rework on hidden devices due to device failure or manufacturing defect.
  3. Test access may become limited.
- The highest degree of manufacturability exists when proper courtyard spacing is utilized.
5.4 SMD Size Requirements and Capabilities.

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Production</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0201</td>
<td>Yes</td>
<td>5,000 per board max.</td>
</tr>
<tr>
<td>Micro BGA</td>
<td>Yes</td>
<td>Less than 54mm²</td>
</tr>
<tr>
<td>PBGA</td>
<td>0.4, 0.5, 0.8 mm</td>
<td>Less than 54mm²</td>
</tr>
<tr>
<td>CBGA</td>
<td>1.0, 1.27, 1.800 balls</td>
<td>Less than 54mm²</td>
</tr>
<tr>
<td>QFN / CSP</td>
<td>32 – 128 I/O, 0.5mm pitch</td>
<td></td>
</tr>
<tr>
<td>Fine Pitch</td>
<td>15.8 – 20mil pitch up to 304 I/O</td>
<td>Capable to 12mil</td>
</tr>
<tr>
<td>CLCC</td>
<td>Yes</td>
<td>Less than 54mm², not to exceed 80grams</td>
</tr>
<tr>
<td>Tray Components</td>
<td>50 stock numbers, 150 trays total</td>
<td></td>
</tr>
</tbody>
</table>

Table 15: SMD size and capabilities.

5.4.1 Resistor Pack (R-Pack) Limitations

Resistor Packs also called R-Packs or Resistor Networks have critical design features that can limit the manufacturability of a PABA and add additional rework time. To improve manufacturability and to limit the number of solder defects associated with resistor packs, it is preferred that the design incorporates resistor packs with Convex type terminations and external solder joints. Convex terminations with external solder joints on resistor packs provide a better surface for improved solder joints and provide easier access to the solder joints for inspection and if necessary rework.

PCBA designs that incorporate resistor packs that incorporate other designs such as castellation-type packages are prone to latten terminal plating issues, solder defects and undetectable internal hairline cracking that cannot be detected.

5.4.2 Thermal Process Requirements for SMD and Through Hole Components (Reflow and Wave Solder)

Surface Mount:
SnPb Eutectic Process – Package Classification Peak Reflow Temperatures:

<table>
<thead>
<tr>
<th>Package Thickness</th>
<th>Volume mm³ &lt;350</th>
<th>Volume mm³ ≥350</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;2.5mm</td>
<td>240 ±0/-5 °C</td>
<td>225 ±0/-5 °C</td>
</tr>
<tr>
<td>≥2.5mm</td>
<td>225 ±0/-5 °C</td>
<td>225 ±0/-5 °C</td>
</tr>
</tbody>
</table>

Table 16: SnPb Eutectic process – package classification reflow temperatures.

Pb-Free Process – Package Classification Reflow Temperatures

<table>
<thead>
<tr>
<th>Package Thickness</th>
<th>Volume mm³ &lt;350</th>
<th>Volume mm³ 350 - 2000</th>
<th>Volume mm³ &gt;2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;1.6 mm</td>
<td>260 ±0 °C</td>
<td>260 ±0 °C</td>
<td>260 ±0 °C</td>
</tr>
<tr>
<td>1.6 mm – 2.5 mm</td>
<td>260 ±0 °C</td>
<td>250 ±0 °C</td>
<td>245 ±0 °C</td>
</tr>
<tr>
<td>≥2.5 mm</td>
<td>250 ±0 °C</td>
<td>245 ±0 °C</td>
<td>245 ±0 °C</td>
</tr>
</tbody>
</table>

Table 17: Lead-free process – package classification reflow temperatures
Figure 16: IPC-0020C Classification reflow profiles for tin-lead and lead free solders.
Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly
--- | --- | ---
Average Ramp-up rate (T_{s, max} to T_p) | 3 °C/Second maximum | 3 °C/Second maximum
Preheat Temperature Min (T_{s, min}) | 100 °C | 150 °C
Temperature Max (T_{s, max}) | 150 °C | 200 °C
Time (t_{s, min} to t_{s, max}) | 60-120 seconds | 60-180 seconds
Time maintained above (liquidus) Temperature (T_L) | 183 °C | 217 °C
Time (t_L) | 60-150 seconds | 60-150 seconds
Peak Classification Temperature (T_p) | See Table 16 | See Table 17
Time within 5 °C of actual Peak Temperature (t_p) | 10-30 seconds | 20-40 seconds
Ramp Down Rate | 6 °C/second maximum | 6 °C/second maximum
Time 25 °C to Peak Temperature | 6 minutes maximum | 8 minutes maximum

Table 18: Classification reflow profile.

Wave Solder Thermal Process:

<table>
<thead>
<tr>
<th></th>
<th>Sn-Pb</th>
<th>Pb-Free</th>
</tr>
</thead>
<tbody>
<tr>
<td>Immersion in Bath</td>
<td>Components must be specified for a minimum temperature of 475 °F for a minimum of 4 seconds and should be specifically designed for immersion in solder bath.</td>
<td>Components must be specified for a minimum temperature of 525 °F for a minimum of 4 seconds and should be specifically designed for immersion in solder bath.</td>
</tr>
<tr>
<td>Plated Through Holes (PTH)</td>
<td>Component leads must be capable of a minimum temperature of 475 °F for a minimum of 4 seconds.</td>
<td>Component leads must be capable of a minimum temperature of 525 °F for a minimum of 4 seconds.</td>
</tr>
<tr>
<td>Top-Side Pre-Heat</td>
<td>Typical Preheat temperatures are 160-260°F. Components must be capable of surviving these pre-heat temperatures.</td>
<td>Typical Preheat temperatures are 200-300°F. Components must be capable of surviving these pre-heat temperatures.</td>
</tr>
</tbody>
</table>

Table 19: Wave solder thermal process.

5.5 Through Hole Components

GUIDELINE
Axial leaded components are preferred over radial leaded components. Directional package style is preferred over bi-directional. This prevents components from being miss-orientated.

Hole Size requirements. Use Table 20 for determining Plated Through Hole (PTH) finished sizes. Use column A to maximize hole tolerances and manufacturability whenever possible.
- PTH too large: Components will “jump” out of board during handling, have reduced parallelism / perpendicularity or increased component lift, may not allow for a topside fillet (inspection aid), flood the topside of the board with solder (from the wave solder machine) creating solder shorts.
- PTH too small: Interference fit may not allow component to fit PTH, may not allow for proper ultrasonic spray fluxing clearances (resulting in insufficient solder fill).
5.6 Thermal Isolation

Thermal isolation is critical to hand soldering, wave soldering and SMT processes. This is especially true on multi-layer, high copper content assemblies. Without this isolation it becomes difficult to maintain process temperatures in the soldering areas of the assembly. The idea here is to slow the rate of heat sinking out of the PTH through the use of isolation (artwork). Utilize IPC-275 where ALL layers contact PTH barrels.

Good isolation techniques yield:
   a. More complete PTH (barrel) fill with solder.
   b. Solder joint inspection is faster / easier.
   c. Greater manufacturability, improved reliability

Poor isolation techniques yield:
   a. Incomplete barrel fill.
   b. Greater difficulty in inspection because of no fillet. No fillet = difficulty in determining barrel fill.
   c. Less manufacturability, lower reliability

5.7 Bar-Code Labels

Bar code labels are added to all assemblies to provide real-time tracking and traceability. Labels can be temporary or can be a permanent fixture of the assembly. Permanent labels are preferred. However, this will require a space on the PCB surface for label attachment.
Label requirements:

Label size is 0.9 x 0.25 inch. Label is 2.5 mil +/- 1.0 mil. Label can survive up to 350 Celsius for 80 seconds. Clearance around the label is a function of surrounding components. Label must remain visible on PCB assembly throughout assembly process.

<table>
<thead>
<tr>
<th>Label Clearance</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal</td>
<td>0.25 inch</td>
</tr>
<tr>
<td>Acceptable</td>
<td>0.1 inch</td>
</tr>
<tr>
<td>Acceptable</td>
<td>0.050 inch</td>
</tr>
</tbody>
</table>

Table 21: Bar code label clearance requirements

6.0 Double Sided Boards

6.1 Back side Wave Soldering (Type II or Type III Assemblies)

Boards designed as double-sided assemblies with components wave soldered on the secondary (back) side. This method is typically only preferred for short production runs. They require special design rules.

The minimum spacing shown below of .025” land to land perpendicular to the solder direction and .025” land to land parallel to the solder direction MUST be maintained to avoid wave solder defects (bridging). The minimum spacing from the edge of the annular ring of through-hole component pads or vias to a surface mount land or another via is .025”.

Figure 17: Chip-in-wave minimum component clearances.

All components used on the wave solder sides of an assembly MUST be approved for immersion in a solder bath.

Components taller than .100” (typically tantalum caps or inductors) require .100” clearance land to land in all directions to prevent solder defects (skips and opens) during the wave solder operation. Components or leads are limited to .125” in height or length to clear the solder pot nozzle in the wave solder machine.
6.2 Back Side Wave Soldering (Type II or Type III Assemblies, continued)

Components that cannot be placed on the backside are as follows:

- BGA components
- CSP components
- QFP components
- "J" leaded devices
- Connectors
- Any device that cannot be submerged in solder.
- Non-encapsulated inductors

6.3 Selective Wave Soldering

Preferred method for processing mixed technology boards. The DFM requirements for this process are different than that of section 6.1. SMD components on the backside of the PCB are reflow soldered. A custom wave solder fixture shields the SMD components from being submerged in to solder. Only the through hole components are left exposed for wave soldering.

The clearance required on the backside of the board from the edge of a through-hole lead is .125". This is to allow sufficient space for the wave solder fixture to shield the SMD components as well as enough clearance to break the surface tension of the solder and allow it to make contact with the through-hole lead. A reduction in clearance will impact the wall thickness of the fixture and/or create a shadowing effect resulting in "open" solder connections.

Figure 18: Mixed Technology component clearances for selective soldering.
Additionally, thinner wall dimensions will reduce the total life expectancy of the solder pallets.

Rule:
- Thicker walls = longer pallet life (greater number of wave solder cycles).
- Thinner walls = lower pallet life (lower number of wave solder cycles).

0.125 inch clearance violations that lead to pallet wall thickness of 0.025 inch will yield extremely short pallet life. If a design cannot yield to these requirements and must survive many thermal excursions, individual pockets (of the wave pallet) can be fitted with titanium inserts. These inserts are very expensive and can increase the cost of a pallet by 30-50% or higher (depending on the number of titanium pockets required per pallet).

The height of SMD components on the backside should not exceed .090". There can be some isolated areas that can exceed this to a maximum height of .120". The cavity in the fixture will be modified in these areas and should not affect the life of the fixture. All parts that exceed these criteria will most likely be hand soldered.

Orientation of the SMD components is not critical in this process.

![Figure 19: SMT component heights for selective soldering.](image)

7.0 Pad Configuration

7.1 Fine Pitch Components (Pitch ≤ 0.025")

The length of the pad should extend .020" away from the toe and heel of the lead itself. The width should be 50-55% of the pitch. These should be non-solder masked defined pads.
7.1 Fine Pitch Components (Pitch ≤ .025”, CONTINUED)

Local fiducial should be positioned in each fine pitch location to improve the placement accuracy of the device. Single fiducial pattern must have fiducial centered within device footprint. Dual fiducial pattern must locate fiducials equally spaced from footprint center (mirror image along both diagonals).
7.2 BGA Components

BGA Pad sizes are dependent on the pitch of the components. The pad geometry should be as follows:

<table>
<thead>
<tr>
<th>Package Type</th>
<th>PCB Pad Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBGA</td>
<td>.0285&quot; +/- .0015&quot;</td>
</tr>
<tr>
<td>1.5 mm pitch PBGA</td>
<td>.025&quot; +/- .001&quot;</td>
</tr>
<tr>
<td>1.27 mm pitch PBGA</td>
<td>.023&quot; +/- .001&quot;</td>
</tr>
<tr>
<td>1.0 mm pitch PBGA</td>
<td>.020&quot; +/- .001&quot;</td>
</tr>
<tr>
<td>.75 mm pitch PBGA</td>
<td>.012&quot; +/- .001&quot;</td>
</tr>
</tbody>
</table>

Table 22: BGA pad size recommendations

The traces that connect vias to BGA pads need to be masked off as a minimum to prevent solder from scavenging into the vias. The BGA pads are non-solder masked defined.

Figure 22: Masked via on BGA pad.
8.0 Surface Mount/Wave Solder Tooling and Stencil Fabrication

Guideline

CAD data is the preferred format of data exchange. The following are the preferred standard CAD data formats used for the design of fixtures and tooling:

- Gerber
  - Basic or Standard Gerber (RS274D) – requires a separate aperture file
  - Extended Gerber (RS274X) – embedded aperture data
- ODB++
  - ODB++ is an intelligent format that captures all the CAD/EDA, assembly and PCB fabrication knowledge in one single database. This format takes the place of individual gerber, drill, and aperture files, and adds additional information that helps produce more accurate, higher quality fixtures.
- FTP (File Transfer Protocol) is the preferred data transfer method over email when data package exceeds 5 MB of file size. Please contact Vanguard for FTP access information.

8.1 Data Requirements:
2. Global fiducials must be incorporated in the paste files.
3. Read me files describing what the Gerber files are.
4. A drawing of the board in AUTOCAD .DWG, .DXF or PDF format is desirable. A drawing in Gerber or HPGL format are also acceptable.
5. A sample board is desirable.
6. If the boards are multiple imaged on an array (flat), a step and repeat drawing of the array layout or GERBER data for the array is required. We would desire this in the same .DWG or .DXF format. A hard copy drawing is an acceptable alternative.

8.2 Stencil Data requirements:
1. Paste, Silkscreen and Mask layer. If PCB is two-sided, data is needed for each side.
2. Silkscreen layer(s) should include reference designators, polarity markings and part outline. Refer to Section 5.4 for more details.
3. PCB outline.
4. Fiducials
5. If more than one image, develop array paste layer(s) and overall PCB layout showing entire PCB with image outlines.
6. Special customer requirements for apertures.

8.3 Tooling Data Requirements:
1. PCB Fabrication Drawing: Gerber, pdf, .dwg, .dxf are acceptable formats
2. Solder mask, Silkscreen, and Paste Gerber layers. Top and bottom as applicable.

9.0 CAD Data Requirements for Placement Programming

9.1 CAD File
A. Ascii Cad: Many Cad/PCB Board Design Software application allow for the export of Cad data in ASCII (text) format. This data can be imported directly into Unicam or Fabmaster at Vanguard to generate SMT machine programs and test programs, respectively.
B. The following are extraction procedure and typical header output of the more popular PCB Design Software. Vanguard can provide instructions for exporting ASCII CAD specific to a CAD/PCB Design Software application:

- Cadence Allegro
- Extraction Procedure:
Cadence Allegro requires the use of a script available from www.aiscorp.com. The script produces a "ccam.cad" file that can then be imported into CircuitCAM.

Common File Extension: "*.cad"

File header:

A Cadence Allegro file can be very easily distinguished by the !marks in the output file. 29 data fields are required in the output file.

- GenCAD v1.4 from Veribest

Extraction Procedure:
Veribest provides a stand-alone application called Report Writer. Use this application to export the "Mitron" export option, which causes Veribest to produce a GenCAD compliant output ASCII file.

Common File Extension: "*.cad"

File Header:
$HEADER
GENCAD 1.4
USER RSI-TRANSLATOR GENCAD OUTPUT V:10
DRAWING scm
UNITS USER 1000
ORIGIN 0 0
INTERTRACK 0
$ENDHEADER

9.2 BOM file

A. File format: Soft copy in ASCII or plain text, comma delimited or tabular. Columnized, Excel format preferred.

B. Description: This file SHOULD provide accurate information on:
1. Customer part numbers.
2. Part Description, which contains the identification of the component itself. This aids in validating that the correct components are issued to the floor. Include part type in description: CBGA, PBGA, SOIC8, etc.
3. Reference Designators.
4. Qty per part number.
5. BOM Notes, which highlight any instructions regarding the part number.
6. Separate DNI (Do Not Install) list. SMT Components identified as "DNI" will not have apertures cut in the solder stencil.
7. See Table 23 for an example of the preferred BOM structure

<table>
<thead>
<tr>
<th>Item Number</th>
<th>Part Description</th>
<th>Ref Des</th>
<th>Qty</th>
<th>BOM Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000016-001</td>
<td>IC 74HC00 QUAD 2 INP</td>
<td>U106, U128, U138, U158</td>
<td>4</td>
<td>No Clean Only</td>
</tr>
<tr>
<td>1000039-001</td>
<td>IC, 74HC245 OCTGAL XCVR</td>
<td>U23A, U23B</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

Table 23 Example of Preferred BOM Structure

1. SILKSCREEN GERBER files (Top and/or Bottom)
**10.0 Mechanical Requirements for PCBA**

**10.1 Torque Requirements for Hardware**

The assembly drawings or assembly instructions should specify the torque requirements for all hardware attached to the PCBA. Examples of hardware needing torque requirements are shown below:

1. Screws for sheet metal
2. Component hold down screws
3. Standoffs
4. Connector hardware and hold down screws
5. Fittings for pneumatic components

Table 23 lists the possible torque values for various types and sizes of screws. It is the customer’s responsibility to evaluate these values and ensure they are proper for the environmental conditions that the assembly is designed for.

**10.2 Self-Clinching Fasteners**

The PCB layout should provide a minimum of 3mm clearance order to have sufficient clearance for tooling used for inserting the Self-Clinching Fastener. In cases where the manufacturer recommends a larger clearance than 3mm, then the manufacturer’s recommendation should be followed. The pad design for the Self-Clinching Fastener should be per the manufacturer’s recommendations including hole size, plating requirements and recommended application.

**10.3 Press Fit connectors**

The PCB layout provides sufficient clearance on the top and bottom side of the PCBA for access for the press fit tooling per the manufacturer’s recommendation. Designs with components placed too close to the press fit connector may require special tooling and fixtures to for proper insertion of the connector.

PCBAs that are thinner than 0.061” will require a base fixture to prevent damaging the board and surrounding components during the press operations.

**11.0 System Integration (box build)**

**11.1 Cosmetic Specifications**

Cosmetic specifications should be provided detailing the criteria of inspection for cosmetic blemishes. The specification should outline the magnification used for inspection, the distance and angle used for inspection.
11.2 Fabricated parts
Drawings should be supplied for all fabricated components. Drawing should include specific information on material, tolerance and finish requirements.

11.3 Assembly Drawings and Work Instructions
Assembly drawings and work instructions should be provided, defining the sequence of the assembly process. Critical aspects related to the building of the product as well as torque specifications for any hardware should be defined. Complex assemblies should have drawings broken into sub-assemblies or the specific build sequence. In the absence of torque specifications Vanguard will default to ASME standard torque table.

11.4 Packaging
Instructions should be supplied illustrating the packaging requirements for the product. These instructions should include all label requirements, foam inserts, literature, box and bag requirements.

Labels, literature and packaging materials should be on the BOM.

In the absence of shipping instructions and customized packaging, Vanguard will default to the following.
1) Supply parts free from all contamination
2) When items are ESD-sensitive, packaging will be ESD safe and labeled appropriately
3) Ship in packaging that ensures adequate protection from mechanical/ESD damage during ordinary handling and shipping.
4) Packaging shall meet the minimum packaging requirement of the common carriers.
## Appendix A – Critical Item DFM Checklist

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Critical Items for Pre-DFM Consideration</th>
<th>DFM Manual Section</th>
<th>Options</th>
</tr>
</thead>
</table>
| 1        | Documentation Requirements: CAD Data Requirements for Placement Programming, BOM format. PCB Spec Dwg (initial review by tech support) | 9                   | 1. Request data from customer  
2. Produce centroid files from GERBER |
| 2        | Board Dimensions: Length, Width, Thickness. Will this fit into a standard process? (max 18x16x0.062) | 4                   | 1. No bid  
2. Hand solder  
3. Outsource build  
4. Special tooling to run on SMT |
| 3        | Fiducials: Size, Features and Locations. Are fiducials present? Correct size / features? Right locations? This includes arrays if the customer is providing the array data | 3.6  
3.3.1 | 1. Request customer to add  
2. Vanguard add array rails/frame to add fiducials  
3. Use alternate features if available  
4. No bid |
| 4        | Manufacturability vs. Form factor (shape). Irregular shape, too small for machine? Array or fixtures required? | 4.7 | 1. Create array layout  
2. Use SMT fixtures |
| 5        | Tooling holes - method for securing boards. This includes arrays if the customer is providing the array data | 4.2  
3.3.1 | 1. Request customer to add holes per DFM manual.  
2. Vanguard add array to add tooling holes  
3. Use edge clamps |
| 6        | SMD Size Requirements and Capabilities. Are these components within our placement capabilities? SMT heights proper for Selective Wave solder? | 5.4 | 1. Hand solder, specify # of leads  
2. Place using SRT  
3. Place in paste  
4. DNI  
5. Use Special tooling |
| 7        | Component Spacing. SMT to SMT spacing. Spacing around BGAs. Can a standard process be used? | 5.2 | 1. Machine place  
2. Hand place in paste  
3. Hand solder, specify # of leads |
| 8        | Plating Recommendations. Is plating appropriate for the assembly technology? | 3.2 | 1. Recommend different plating  
2. Run as is |
| 9        | Double Sided Assemblies for Wave Solder. Th-to-SMT spacing for standard process? | 6 | 1. Hand solder, specify # of leads  
2. Titanium Wave Fixtures |
| 10       | De-panel / Tab Routing Guidelines. Can we de-panel this? V-score or mouse bite. Parts too close to de-panel features. | 4.3 | 1. Request customer change type &/or placement of de-panel design  
2. Hand solder parts close to de-tab  
3. Use router to de-tab |
| 11       | Component spacing around PEMs. PEM diameter +3mm (minimum) spacing. | 10.2 | 1. Recommend customer change spacing  
2. Component to be hand soldered  
3. Custom tool required |
Appendix B – Best Practice - Small Chip Layout

0201 and 0402 Pad Spacing and Length

Pad width is not shown but should be .012” for 0201s and .022” for 0402s.

Appendix C – Best Practice – AL Cap Layout

Electrolytic Capacitor Layout

SMT Electrolytic Capacitors require spacing between adjacent placements.

A common issue with electrolytic capacitors is that the leads are often off-center from the base plate. See Figure 1. This exaggerates the spacing issue as placement vision systems use the leads to align the parts.

At least 1.00mm space is recommended between electrolytic capacitors to prevent collisions between component bases during automated placement. Figure 2 shows a negative example of no spacing between components.
Appendix D – Best Practice – D-Pak Layout

D-pak Layout

D-paks consistently float during reflow and settle where the thermal tab aligns very close to the pad edge. Extending signal pads allows space for the component dimensional tolerance and component movement.

Overlay view

Original pad length is too short. No heel fillet exists with part at lower spec.

Appendix E – Best Practice – LFPAK Layout

LFPAK DFM

The LFPAK design creates an air pocket in the un-plated region of the thermal tab. During the second reflow pass, gravity works together with an explosion of the trapped air pocket. The results range from a blow hole to the part being ejected from the surface of the assembled. Vanguard has done extensive research on this issue and has designed a layout that provides an outgassing channel.

Vanguard observed the following failure modes using the inferior pad design.

1. Fracture Arrest, Vapor Welding, Thermal Tab, Fracture Initiation, Lead Section
2. Vapor Welding, Hot Fluid Flux, Fracture Initiation, Lead Section
3. Fracture Arrest, Hot Fluid Oxidation, Oxidation Fracture, Lead Section
4. Fracture Arrest, Vapor Welding, Lead Section, Oxidation Fracture, Lead Section
5. Fracture Arrest, Vapor Welding, Lead Section, Oxidation Fracture, Lead Section
6. Fracture Arrest, Vapor Welding, Lead Section, Oxidation Fracture, Lead Section
Appendix F – Best Practice – SMT PEM Paste Layer

SMT Standoff/PEM Nut Design Recommendations
(Graphics not to scale)

Most paste layers do not contain apertures that deliver enough paste to SMT Standoff or PEM devices. Shown is an example of the change in paste volume needed to produce an IPC compliant solder joint.

NOTE: No generic recommendations are given for changes to the pads. Diameter recommendation is in relation to pad size, but only applies to the Paste layer.